FEDL7214_001DIGEST-P
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OKI Semiconductor

ML7214-001

VoIP CODEC

GENERAL DESCRIPTION

The ML7214-001 that is G.711(μ-law) and G.711(A-law) selectable is a voice CODEC for VoIP including two channels of the Speech CODEC which supports the PLC (Packet Loss Concealment) function. Provided with an echo canceler handling 32 ms delay, FSK generation, DTMF detection/generation, and tone detection/generation functions for each channel, the ML7214-001 is ideally suited for adding the VoIP function to TAs and Routers.

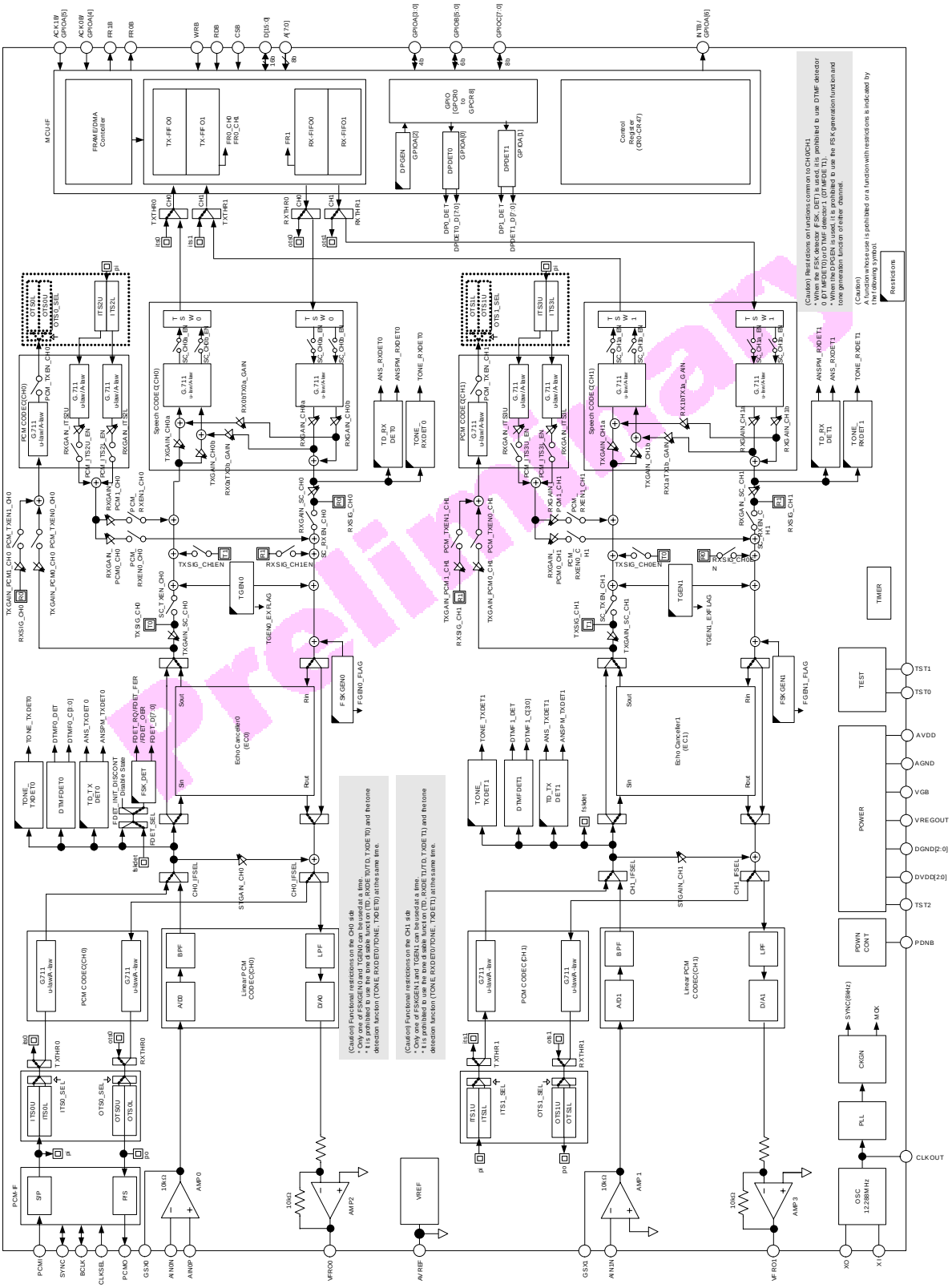
FEATURES

- Speech CODEC (2 channels included)
  - ITU-T G.711 (64 kbps) μ-law and A-law selectable
  - Supports ITU-T G.711 Appendix 1 compliant PLC (Packet Loss Concealment) function
  - Supports the function for handling 2 channels for 3-way speech
- Built-in FIFO buffer for transferring transmit and receive data
  - Interface count: 1 (CH0 and CH1 common)
  - FIFO buffer size: 640 bytes
  - Frame and DMA (slave) interface selectable
- PCM interface
  - Interface count: 1 (CH0 and CH1 common)
  - Coding format: ITU-T G.711 (64 kbps) μ-law and A-law selectable
  - Serial transmission rate: 128 kHz to 2.048 MHz (Fixed to 2.048 MHz when output)
  - 1 time slot bit width: Fixed to 16 bits (upper 8-bit/lower 8-bit selection function)
  - Time slot assignment: Supports up to 16 slots (BCLK: 2.048 MHz)
  - Input time slot selection: any 2 slots selectable in each channel
  - Output time slot selection: any 1 slot selectable in each channel
- Terminal side interface
  Analog or PCM interface selectable
- Analog interface
  Includes 1 unit of input amplifier and 1 unit of output amplifier in each channel (10 kΩdrive)
- Linear PCM CODEC (1 unit included in each channel)
- Echo canceler handling 32ms delay and Comfort Noise generation function (1 unit included in each channel)
- DTMF detection function (1 unit included in each channel)
- DTMF generation function (1 unit included in each channel: Tone generation function allows DTMF signals to be generated)
- 2100 Hz single tone/phase inversion detection function (2 units included in each channel)
- Tone detection function: (400 Hz: 2 units included in each channel. Detection frequency can be changed)
- Tone generation function (1 unit included in each channel)
- FSK generation function (1 unit included in each channel)
- FSK detection function (1 unit included)
- Dial pulse detection function (1 unit included in each channel)
- Dial pulse transmit function (1 unit included)
- 16-bit timer (1 unit included)
- PCM data transparency mode
- General-purpose I/O ports
  21 ports (Secondary functions are assigned to some of the ports)

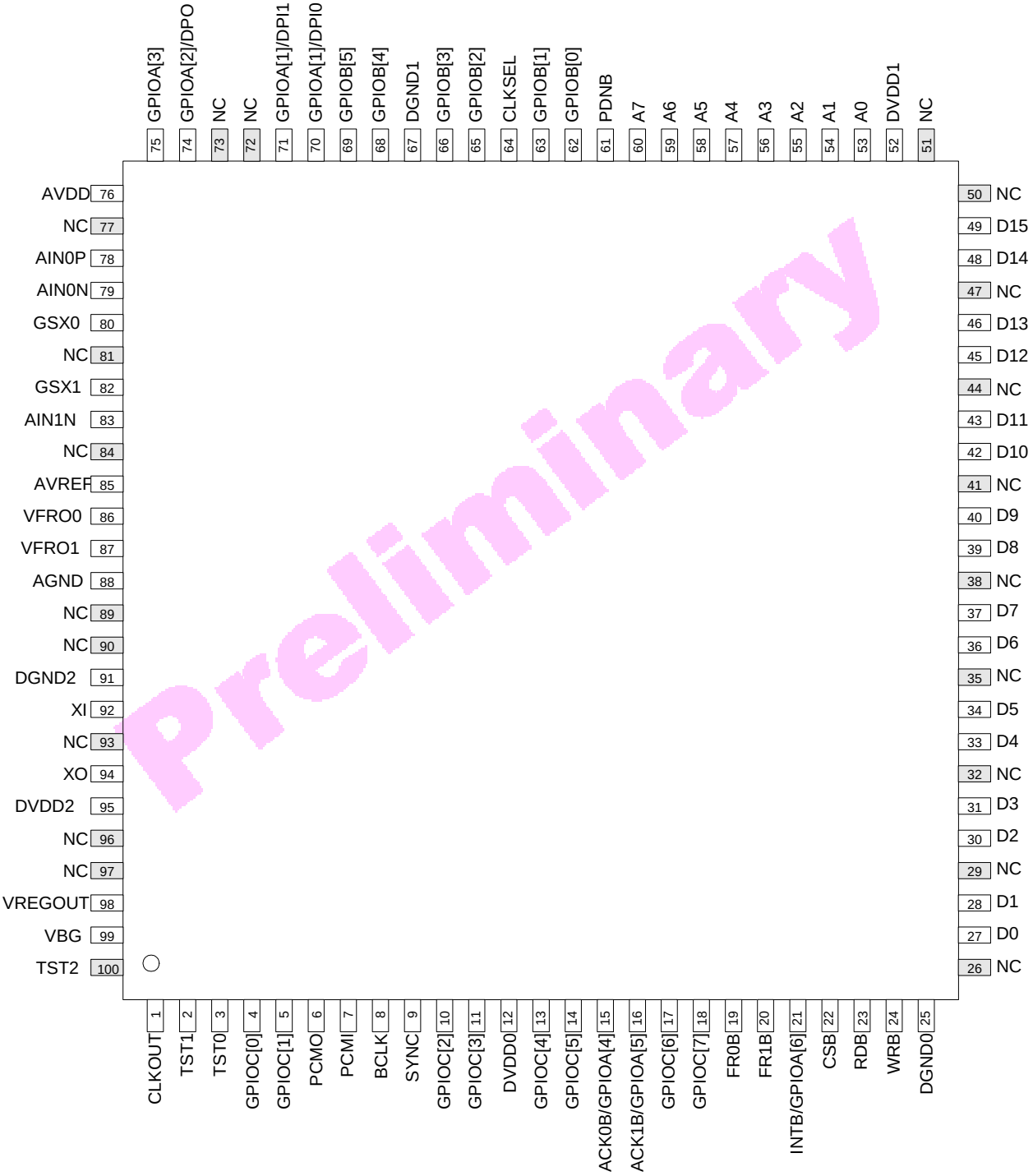
- Power supply:
  - Digital power supply voltage (DVDD0, 1, 2) 3.0 to 3.6 V
  - Analog power supply voltage(AVDD) 3.0 to 3.6 V
- Master clock frequency:
  - 12.288 MHz (crystal/external input)
- Hardware and software power-down
- Package:
  - 100-pin plastic TQFP (TQFP100-P-1414-0.50-K) (ML7214-001TB)

(Note) Some functions are restricted on use. For details, refer to the “NOTES ON USE” Section.

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



100-Pin Plastic TQFP

PIN DESCRIPTIONS

Pin	Symbol	I/O	When PDNB = “0”	Description
1	CLKOUT	O	“L”	12.288 MHz clock output
2	TST1	I	“0”	Test control input 1: Normally, input “0”.
3	TST0	I	“0”	Test control input 0: Normally, input “0”.
4	GPIOC[0]	I/O	I	General-purpose I/O port C [0]
5	GPIOC[1]	I/O	I	General-purpose I/O port C [1]
6	PCMO	O	“Hi-z”	PCM data output [Open drain output pin]
7	PCMI	I	I	PCM data input
8	BCLK	I/O	I	CLKSEL = “0” PCM shift clock input (128 kHz to 2.048 MHz)
			“L”	CLKSEL = “1” PCM shift clock output (2.048 MHz)
9	SYNC	I/O	I	CLKSEL = “0” PCM synchronous signal 8 kHz input
			“L”	CLKSEL = “1” PCM synchronous signal 8 kHz output
10	GPIOC[2]	I/O	I	General-purpose I/O port C[2]
11	GPIOC[3]	I/O	I	General-purpose I/O port C[3]
12	DVDD0	—	—	Digital power supply
13	GPIOC[4]	I/O	I	General-purpose I/O port C[4]
14	GPIOC[5]	I/O	I	General-purpose I/O port C[5]
15	ACK0B/GPIOA[4]	I/O	I	Transmit buffer DMA access acknowledge signal input (primary function) General-purpose I/O port A[4] (secondary function) [5 V tolerant pin]
16	ACK1B/GPIOA[5]	I/O	I	Receive buffer DMA access acknowledge signal input (primary function) General-purpose I/O port A [5] (secondary function) [5 V tolerant pin]
17	GPIOC[6]	I/O	I	General-purpose I/O port C [6]
18	GPIOC[7]	I/O	I	General-purpose I/O port C [7]
19	FR0B (DMARQ0B)	O	“H”	FR0B:(FD_SEL = “0”) Transmit buffer frame signal output DMARQ0B: (FD_SEL = “1”) Transmit buffer DMA access request signal
20	FR1B (DMARQ1B)	O	“H”	FR1B: (FD_SEL = “0”) Receive buffer frame signal output DMARQ1B: (FD_SEL = “1”) Receive buffer DMA access request signal output
21	INTB/GPIOA[6]	I/O	“H”	Interrupt request output (primary function) General-purpose I/O port A [6] (secondary function) [5 V tolerant pin]
22	CSB	I	I	Chip select control input
23	RDB	I	I	Read control input
24	WRB	I	I	Write control input
25	DGND0	—	—	Digital ground (0.0 V)

Pin	Symbol	I/O	When PDNB = “0”	Description
26	NC	—	—	(Unused) Leave this pin open.
27	D0	I/O	I	Data input-output
28	D1	I/O	I	Data input-output
29	NC	—	—	(Unused) Leave this pin open.
30	D2	I/O	I	Data input-output
31	D3	I/O	I	Data input-output
32	NC	—	—	(Unused) Leave this pin open.
33	D4	I/O	I	Data input-output
34	D5	I/O	I	Data input-output
35	NC	—	—	(Unused) Leave this pin open.
36	D6	I/O	I	Data input-output
37	D7	I/O	I	Data input-output
38	NC	—	—	(Unused) Leave this pin open.
39	D8	I/O	I	Data input-output. Fix the input to “L” or “H” when using the pin in 8-bit bus access (BW_SEL = “1”).
40	D9	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = “1”).
41	NC	—	—	(Unused) Leave this pin open.
42	D10	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = “1”).
43	D11	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = “1”).
44	NC	—	—	(Unused) Leave this pin open.
45	D12	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = “1”).
46	D13	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = “1”).
47	NC	—	—	(Unused) Leave this pin open.
48	D14	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = “1”).
49	D15	I/O	I	Data input-output. Fix the input “L” or “H” when using the pin in 8-bit bus access (BW_SEL = “1”).
50	NC	—	—	(Unused) Leave this pin open.
51	NC	—	—	(Unused) Leave this pin open.
52	DVDD1	—	—	Digital power supply
53	A0	I	I	Address input
54	A1	I	I	Address input
55	A2	I	I	Address input
56	A3	I	I	Address input
57	A4	I	I	Address input
58	A5	I	I	Address input
59	A6	I	I	Address input
60	A7	I	I	Address input

Pin	Symbol	I/O	When PDNB = “0”	Description
61	PDNB	I	“0”	Power-down input “0”: Power-down reset “1”: Normal operation
62	GPIOB[0]	I/O	I	General-purpose I/O port B[0]
63	GPIOB[1]	I/O	I	General-purpose I/O port B[1]
64	CLKSEL	I	I	SYNC/BCLK input-output control input “0”: SYNC/BCLK are configured to be input “1”: SYNC/BCLK are configured to be output
65	GPIOB[2]	I/O	I	General-purpose I/O port B[2]
66	GPIOB[3]	I/O	I	General-purpose I/O port B[3]
67	DGND1	—	—	Digital ground (0.0 V)
68	GPIOB[4]	I/O	I	General-purpose I/O port B[4]
69	GPIOB[5]	I/O	I	General-purpose I/O port B[5]
70	GPIOA[0]/DPI0	I/O	I	General-purpose I/O port A[0] [5 V tolerant pin]/ input pin 0 for dial pulse detection
71	GPIOA[1]/DPI1	I/O	I	General-purpose I/O port A[1] [5 V tolerant pin]/ input pin 1 for dial pulse detection
72	NC	—	—	(Unused) Leave this pin open.
73	NC	—	—	(Unused) Leave this pin open.
74	GPIOA[2]/DPO	I/O	I	General-purpose I/O port A[2] [5 V tolerant pin] Secondary function: Output pin for dial pulse transmission
75	GPIOA[3]	I/O	I	General-purpose I/O port A[3] [5 V tolerant pin]
76	AVDD	—	—	Analog power supply
77	NC	—	—	(Unused) Leave this pin open.
78	AIN0P	I	I	AMP0 non-inverting input
79	AIN0N	I	I	AMP0 inverted input
80	GSX0	O	“Hi-z”	AMP0 output (10 kΩ driving)
81	NC	—	—	(Unused) Leave this pin open.
82	GSX1	O	“Hi-z”	AMP1 output (10 kΩ driving)
83	AIN1N	I	I	AMP1 inverted input
84	NC	—	—	(Unused) Leave this pin open.
85	AVREF	O	“L”	Analog signal ground (1.4 V)
86	VFRO0	O	“Hi-z”	AMP2 output (10 kΩ driving)
87	VFRO1	O	“Hi-z”	AMP3 output (10 kΩ driving)
88	AGND	—	—	Analog ground (0.0 V)
89	NC	—	—	(Unused) Leave this pin open.
90	NC	—	—	(Unused) Leave this pin open.
91	DGND2	—	—	Digital ground (0.0 V)
92	XI	I	I	12.288 MHz crystal interface, 12.288 MHz clock input
93	NC	—	—	(Unused) Leave this pin open.
94	XO	O	“H”	12.288 MHz crystal interface

Pin	Symbol	I/O	When PDNB = “0”	Description
95	DVDD2	—	—	Digital power supply
96	NC	—	—	(Unused) Leave this pin open.
97	NC	—	—	(Unused) Leave this pin open.
98	VREGOUT	—	—	Internal regulator voltage output pin (approx. 2.5 V)
99	VBG	—	—	Internal regulator reference voltage output pin
100	TST2	I	“0”	Test control input 2. Normally input “0” to this pin.

* Explanation of symbols used in the PDNB = “0” column

The symbols denote the following pin conditions when PDNB = “0”:

“I” : Input a High or Low level signal to the pin.
“0” : Input a Low level signal to the pin
“H” : A High level signal is output from the pin.
“L” : A Low level signal is output from the pin.
“Hi-Z” : The pin goes into a Hi-Z state.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition		Rating	Unit
Analog power supply voltage	AVDD	—		–0.3 to +4.6	V
Digital power supply voltage	DVDD	—		–0.3 to +4.6	V
Analog input voltage	VAIN	Analog pin		–0.3 to AVDD+0.3	V
Digital input voltage	VDIN1	Normal digital pin		–0.3 to DVDD+0.3	V
	VDIN2	5 V tolerant pin	DVDD = 3.0 to 3.6 V	–0.3 to +6.0	V
			DVDD < 3.0 V	–0.3 to DVDD+0.3	V
Output current	IO	—		–20 to +20	mA
Power dissipation	PD	Ta = 60 °C, per package		350	mW
Storage temperature	Tstg	—		–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog power supply voltage	AVDD	—	3.0	3.3	3.6	V
Digital power supply voltage	DVDD	—	3.0	3.3	3.6	V
Operating temperature range	Ta	—	–20	—	+60	°C
Digital high-level input voltage	VIH1	Normal digital pin	0.75 × DVDD	—	DVDD+ 0.3	V
	VIH2	5 V tolerant pin	0.75 × DVDD	—	5.5	V
Digital low-level input voltage	VIL	Digital pin	–0.3	—	0.19 × DVDD	V
Digital input rise time	tIR	Digital pin	—	2	20	ns
Digital input fall time	tIF	Digital pin	—	2	20	ns
Digital output load capacitance	CDL	Digital pin	—	—	50	pF
Digital output load resistance	RDL	Pull-up resistance, PCMO	500	—	—	Ω
AVREF bypass capacitor	Cvref	Between AVREF-AGND	2.2+0.1	—	4.7+0.1	µF
VREGOUT bypass capacitor	Cvout	Between VREGOUT-DGND	—	10+0.1	—	µF
VBG bypass capacitor	CVBG	Between VBG-DGND	—	150	—	pF
Master clock frequency	Fmck	MCK	–0.01%	12.288	+0.01%	MHz
PCM shift clock frequency	Fbclk	BCLK (at input)	128 (±0.1%)	—	2048 (±0.1%)	kHz
PCM synchronous signal frequency	Fsync	SYNC (at input)	–0.1%	8.0	+0.1%	kHz
Clock duty ratio	DRCLK	MCK, BCLK (at input)	40	50	60	%
PCM synchronous timing	tBS	BCLK to SYNC (at input)	100	—	—	ns
	tSB	SYNC to BCLK (at input)	100	—	—	ns
PCM synchronous signal width	tWS	SYNC (at input)	1BCLK	—	100	µs

(Note) On power-on/shut-down sequence

For the analog power supply voltage (AVDD) and the digital power supply voltage (DVDD) to be supplied to this LSI, it is recommended that power be applied to them simultaneously. However, if simultaneous power-up is difficult due to the power supply circuit configuration, power them up in the order of DVDD → AVDD.

The power supplies should be shut down in the reverse order of power-on sequence.

ELECTRICAL CHARACTERISTICS

DC Characteristics

(AVDD = 3.0 to 3.6V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply current	ISS	Standby state (PDNB = "0", DVDD = AVDD=3.3 V, Ta = 25°C)	—	200	500	μA
	IDD1	1 channel operating state. Speech CODEC(CH0) start (SC_CH0a EN="1") PCM-IF stop (PCMO0_EN=PCMO1_EN="0" PCMI2_EN=PCMI3_EN="0") Terminal side: Analog IF (AFE0_EN="0", AFE1_EN="1") A 12.288 MHz crystal is connected to XI and XO. The general-purpose I/O ports are in the "H" input state.	—	45	55	mA
	IDD2	2 channel operating state Speech CODEC(CH0/CH1) start (SC_CH0a EN=SC_CH1a EN="1") PCM-IF start (PCMO0_EN=PCMO1_EN="1" PCMI2_EN=PCMI3_EN="1") Terminal side: Analog IF (AFE0_EN="0", AFE1_EN="0") A 12.288 MHz crystal is connected to XI and XO. The general-purpose I/O ports are in the "H" input state.	—	50	65	mA
Digital input pin Input leakage current	IIH	Vin = DVDD	—	0.01	10	μA
	IIL	Vin = DGND	–10	–0.01	—	μA
Digital I/O pin Output leakage current	IOZH	Vou = DVDD	—	0.01	10	μA
	IOZL	Vout = DGND	–10	—	—	μA
High-level output voltage	VOH	Digital input pins, I/O pin IOH = 4.0 mA IOH = 0.5 mA (XO pin) IOH = 1 2.0 mA (CLKOUT pin)	0.78 × DVDD	—	—	V
Low-level output voltage	VOL1	Digital output pins, I/O pin IOL = –4.0 mA IOL = –0.5 mA (XO pin) IO = –12.0 mA (CLKOUT pin)	—	—	0.4	V
	VOL2	Open drain output pins IOL = –12.0 mA	—	—	0.4	V
	VOL3	General-purpose I/O pins *1 IOL = –7.0mA	—	—	0.5	V
Input capacitance (*2)	CIN1	Input pins	—	6	—	pF
	CIN2	I/O pins	—	10	—	pF

*1 The maximum number of pins that can be driven simultaneously at 7mA is seven for the general-purpose I/O pins (GPIOA[6:0], GPIOB[5:0], GPIOC[7:0]).

*2 Design guaranteed value

Analog Interface

(AVDD = 3.0 to 3.6 V, DVDD0, 1 ,2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input resistance (*1)	RIN	AIN0N, AIN0P, AIN1N	10	—	—	MΩ
Output load resistance	RL	GSX0, GSX1, VFRO0, VFRO1	10	—	—	kΩ
Output load capacitance	CL	Analog output pins	—	—	50	pF
Offset voltage	VOF	VFRO0, VFRO1	–40	—	+40	mV
Output voltage level (*2)	VO	GSX0, GSX1, VFRO0, VFRO1 RL = 10kΩ, AMP input 1.3 Vpp	1.158	1.3	1.458	Vpp

*1 Design guaranteed value

*2 –7.7 dBm (600Ω) = 0 dBm0, +3.17 dBm0 = 1.3 Vpp

AC Characteristics in Speech CODEC = G.711 (μ-law) Mode

(AVDD = 3.0 to 3.6V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
		Frequency (Hz)	Level (dBm0)				
Transmit frequency characteristics	LT1	0 to 60	0	25	—	—	dB
	LT2	300 to 3000		–0.15	—	0.20	dB
	LT3	1020		Reference			—
	LT4	3300		–0.15	—	0.80	dB
	LT5	3400		0	—	0.80	dB
	LT6	3968.75		13	—	—	dB
Receive frequency characteristics	LR2	0 to 3000	0	–0.15	—	0.20	dB
	LR3	1020		Reference			—
	LR4	3300		–0.15	—	0.80	dB
	LR5	3400		0	—	0.80	dB
	LR6	3968.75		13	—	—	dB
Transmit signal-to-noise ratio (*1)	SDT1	1020	3	35	—	—	dBp
	SDT2		0	35	—	—	dBp
	SDT3		–30	35	—	—	dBp
	SDT4		–40	28	—	—	dBp
	SDT5		–45	23	—	—	dBp
Receive signal-to-noise ratio (*1)	SDR1	1020	3	35	—	—	dBp
	SDR2		0	35	—	—	dBp
	SDR3		–30	35	—	—	dBp
	SDR4		–40	28	—	—	dBp
	SDR5		–45	23	—	—	dBp
Transmit inter-level loss errors	GTT1	1020	3	–0.2	—	0.2	dB
	GTT2		–10	Reference			—
	GTT3		–40	–0.2	—	0.2	dB
	GTT4		–50	–0.6	—	0.6	dB
	GTT5		–55	–1.2	—	1.2	dB
Receive inter-level loss errors	GTR1	1020	3	–0.2	—	0.2	dB
	GTR2		–10	Reference			—
	GTR3		–40	–0.2	—	0.2	dB
	GTR4		–50	–0.6	—	0.6	dB
	GTR5		–55	–1.2	—	1.2	dB
Idle channel noise (*1)	NIDLT	—	Analog input = AVREF	—	—	–70	dBm0p
	NIDLR	—	PCMI = "1"	—	—	–70	dBm0p
Transmit absolute level (*2)	AVT	1020	0	0.285	0.320	0.359	Vrms
Receive absolute level (*2)	AVR	1020	0	0.285	0.320	0.359	Vrms

*1 P-message weighted filter used

*2 0.320 Vrms = 0 dBm0 = –7.7 dBm (600Ω)

AC Characteristics (Gain Setting) in Speech CODEC = G.711 (μ-law) mode

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Transmit/receive gain setting accuracy	GAC	For all gain set values	–1.0	—	1.0	dB

AC Characteristics (Tone Output) in Speech CODEC = G.711 (μ-law) Mode

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency deviation	fDFT	For all frequency set values	–1.5	—	1.5	%
Output level	oLEV	For all gain set values	–2.0	—	2.0	dB

AC characteristics (DTMF Detector and Other Detectors) in Speech CODEC = G.711 (μ-law) Mode

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

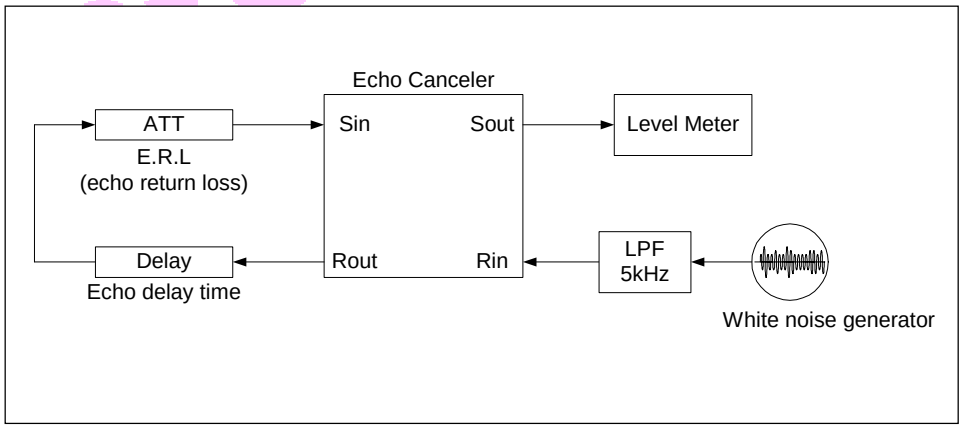
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection level accuracy	dLAC	For all detection level set values	–2.5	—	2.5	dB

AC characteristics (Echo Canceler)

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Echo attenuation	eRES	—	—	35	—	dB
Erasable echo delay time	tECT	—	—	—	32	ms

Measuring method



Timings of PDNB, XO, and AVREF

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-down signal pulse width	tPDNB	PDNB pin	250	—	—	µs
AVDD supply delay time	tAVDDON	—	0	—	—	ns
Oscillation activation time	txtal	—	—	—	20	ms
AVREF rise time	tAVREF	AVREF = 1.4 (90%) C5 = 4.7 µF, C6 = 0.1 µF (See Figure 9)	—	—	600	ms
		AVREF = 1.4 (90%) C5 = 2.2 µF, C6 = 0.1 µF (See Figure 9)	—	—	300	ms

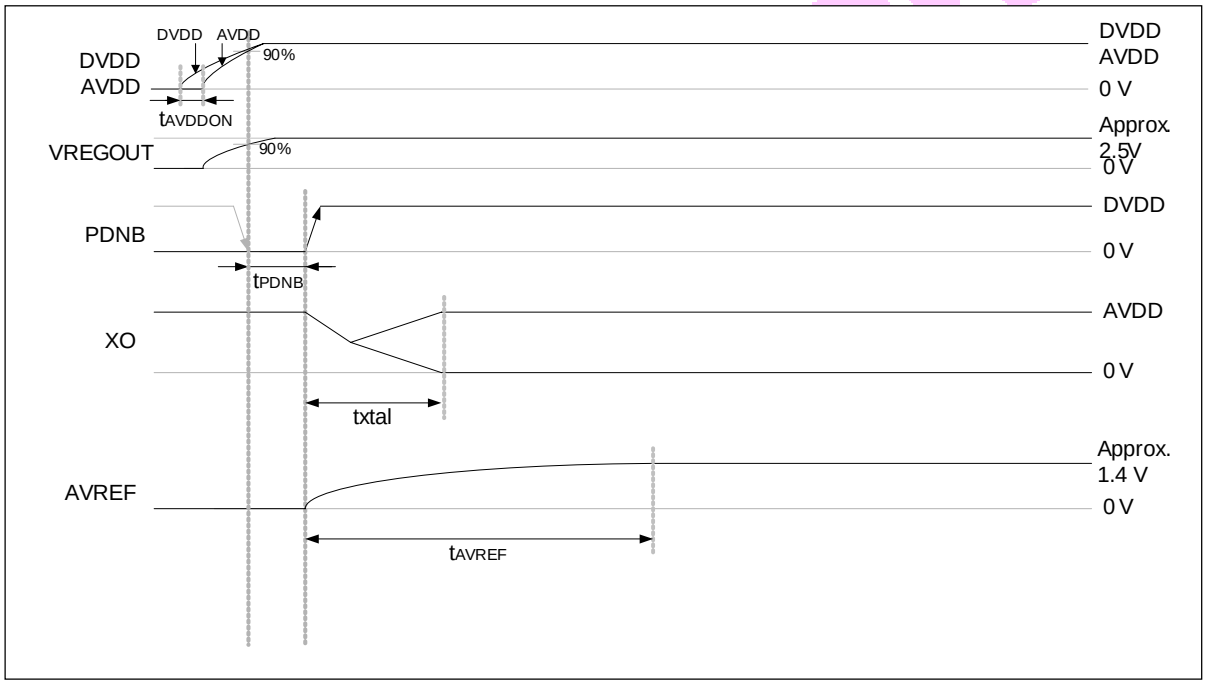


Figure 1 Timings of PDNB, XO, and AVREF

(Note)
The capacitance of the AVREF capacitor (C5) affects the AVREF rise time and analog characteristics. If weight is given to the analog characteristics, specify 4.7 µF, and if it is given to the AVREF rise time, specify 2.2 µF. The electrical characteristics for the analog characteristics that are described above are guaranteed in both capacitances.

PCM interface

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Bit clock frequency (Note)	fBCLK	CDL = 20 pF (during output)	–0.1%	2.048	+0.1%	MHz
Bit clock duty ratio (Note)	dBCLK	CDL = 20 pF (during output)	45	50	55	%
Synchronous signal frequency	fSYNC	CDL = 20 pF (during output)	–0.1%	8	+0.1%	kHz
Synchronous signal duty ratio	dSYNC1	CDL = 20 pF (during output) BCLK = 2.048 MHz At output	45	50	55	%
Transmit/receive synchronous timing	tBS	BCLK to SYNC (during output)	100	—	—	ns
	tSB	SYNC to BCLK (during output)	100	—	—	ns
Input setup time	tDS	PCMI pin	50	—	—	ns
Input hold time	tDH		50	—	—	ns
Digital output delay time	tSDX	PCMO pin Pull-up resistor RDL = 500Ω CDL = 50 pF	—	—	100	ns
	tXD1		—	—	100	ns
Digital output hold time	tXD2		—	—	100	ns
	tXD3		—	—	100	ns

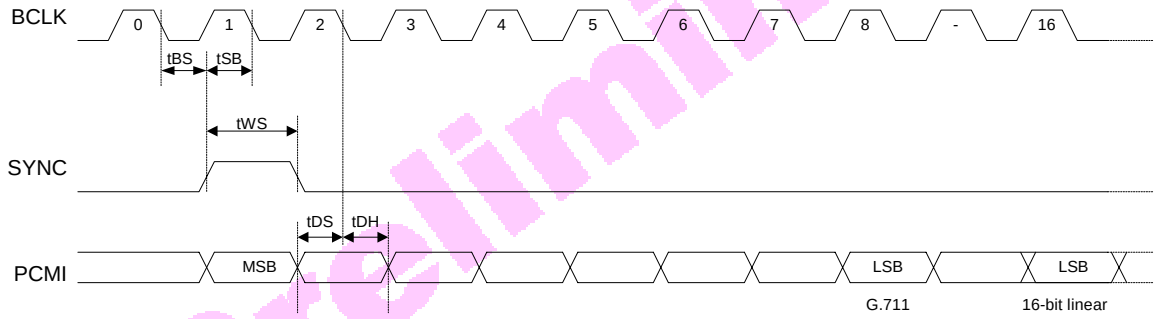


Figure 2 PCM Interface Input Timing (Long Frame)

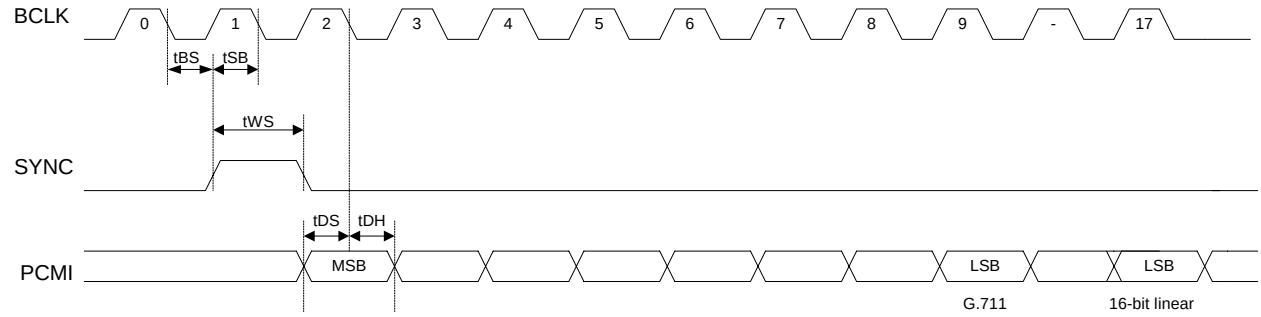


Figure 3 PCM Interface Input Timing (Short Frame)

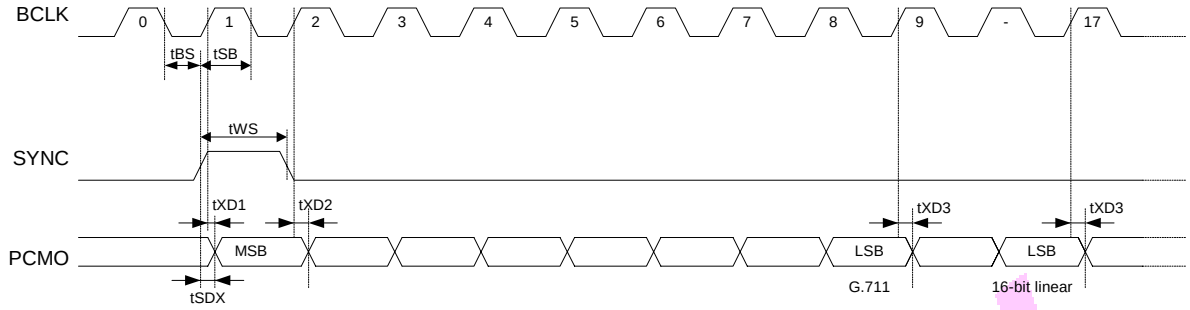


Figure 4 PCM Interface Output Timing (Long Frame)

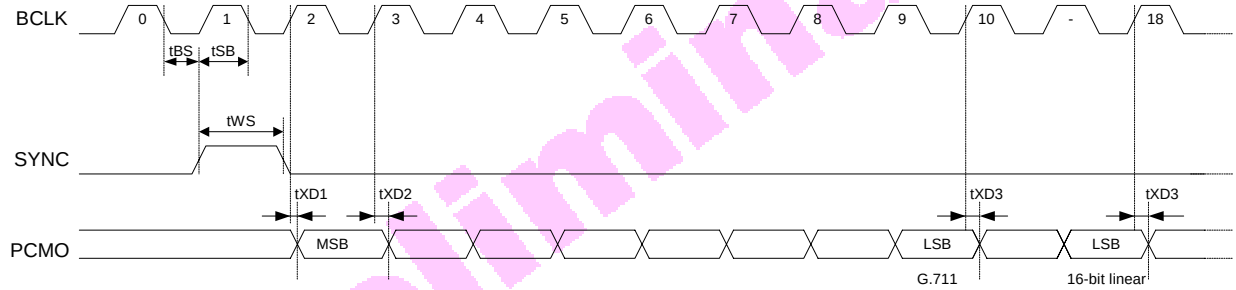


Figure 5 PCM Interface Output Timing (Short Frame)

Control Register Interface

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta= –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Address setup time (at Read)	tRAS	CL = 50 pF	10	—	—	ns
Address hold time (at Read)	tRAH		0	—	—	ns
Address setup time (at Write)	tWAS		10	—	—	ns
Address hold time (at Write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time (at Read)	tRCS		10	—	—	ns
CSB hold time (at Read)	tRCH		0	—	—	ns
CSB setup time (at Write)	tWCS		10	—	—	ns
CSB hold time (at Write)	tWCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
Read data output delay time	tRDD		—	—	20	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		25	—	—	ns
CSB disable time	tCD		10	—	—	ns

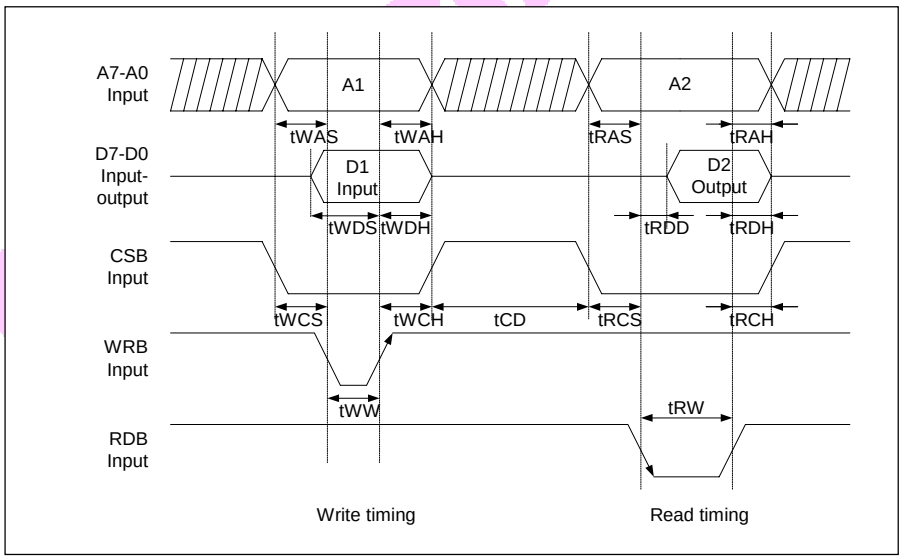


Figure 6 Control Register Interface

Transmit/Receive Buffer Interface (Frame Mode)

(AVDD = 3.0 to 3.6 V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
FR1B setup time	tF1S	CL = 50 pF	3	—	—	ns
FR1B output delay time	tF1D		—	—	20	ns
Address setup time (at Read)	tRAS		10	—	—	ns
Address hold time (at Read)	tRAH		0	—	—	ns
Address setup time (at Write)	tWAS		10	—	—	ns
Address hold time (at Write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
CSB setup time (at Read)	tRCS		10	—	—	ns
CSB hold time (at Read)	tRCH		0	—	—	ns
CSB setup time (at Write)	tWCS		10	—	—	ns
CSB hold time (at Write)	tWCH		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
FR0B setup time	tF0S		3	—	—	ns
FR0B output delay time	tF0D		—	—	20	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
CSB disable time	tCD		10	—	—	ns

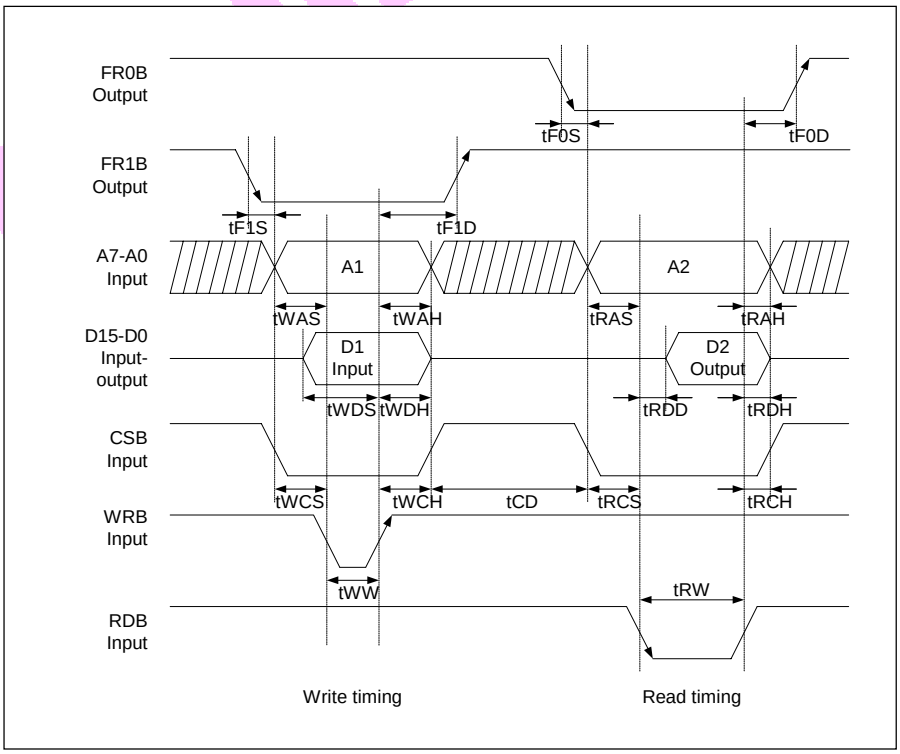


Figure 7 Transmit/Receive Buffer Interface (Frame Mode)

Transmit/Receive Buffer Interface (DMA Mode)

(AVDD = 3.0 to 3.6V, DVDD0, 1, 2 = 3.0 to 3.6 V, AGND = DGND0, 1, 2 = 0.0 V, Ta = –20 to 60°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
DMARQ1B setup time	tDR1S	CL = 50 pF	3	—	—	ns
DMARQ1B output delay time	tDR1RD		—	—	30	ns
	tDR1FD		—	—	30	ns
Address setup time (at Read)	tRAS		10	—	—	ns
Address hold time (at Read)	tRAH		0	—	—	ns
Address setup time (at Write)	tWAS		10	—	—	ns
Address hold time (at Write)	tWAH		10	—	—	ns
Write data setup time	tWDS		20	—	—	ns
Write data hold time	tWDH		10	—	—	ns
ACK0B setup time	tAK0S		10	—	—	ns
ACK0B hold time	tAK0H		0	—	—	ns
ACK1B setup time	tAK1S		10	—	—	ns
ACK1B hold time	tAK1H		10	—	—	ns
WRB pulse width	tWW		10	—	—	ns
DMARQ0B setup time	tDR0S		3	—	—	ns
DMARQ0B output delay time	tDR0RD		—	—	30	ns
	tDR0FD		—	—	30	ns
Read data output delay time	tRDD		—	—	30	ns
Read data output hold time	tRDH		3	—	—	ns
RDB pulse width	tRW		35	—	—	ns
ACKB disable time	tAD		10	—	—	ns

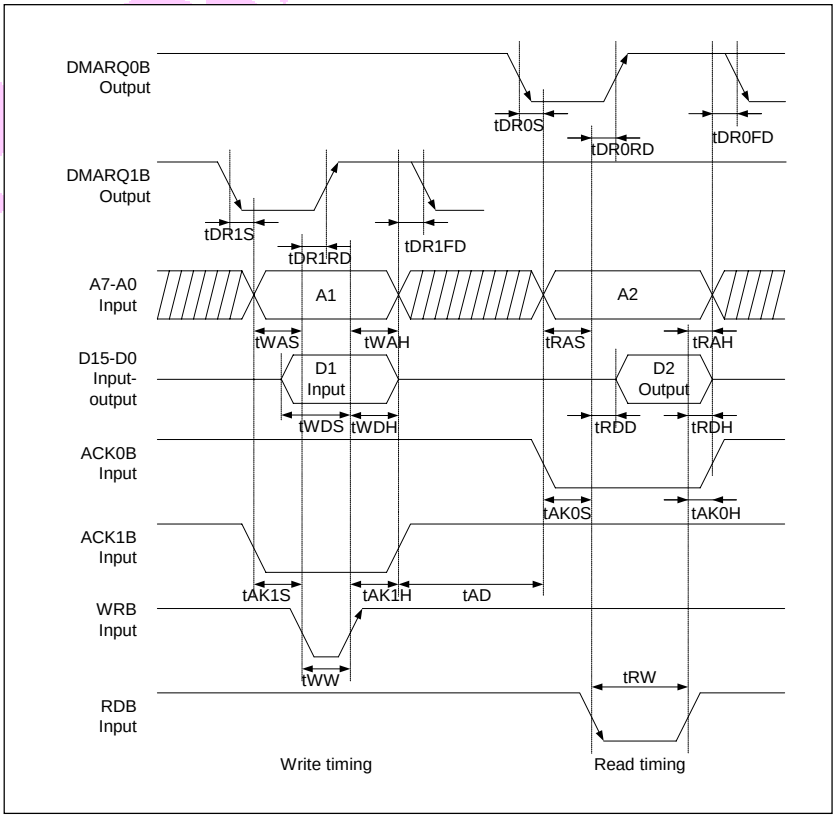


Figure 8 Transmit/Receive Buffer Interface (DMA Mode)

PIN FUNCTIONAL DESCRIPTION

AIN0N, AIN0P, GSX0, AIN1N, and GSX1

These are transmit analog input and transmit gain adjustment pins. AIN0N and AIN1N are connected to inverted input pins of internal transmission amplifiers AMP0 and AMP1, and AIN0P is connected to a noninverting input pin of AMP0. GSX0 and GSX1 are connected to output pins of AMP0 and AMP1. See Figure 9 for the gain adjustment.

At power down (PDNB = "0" or SPDN = "1"), outputs of GSX0 and GSX1 are in a high impedance state. When the application does not use AMP0, short-circuit GSX0 and AIN0N and connect AIN0P with AVREF. When not using AMP1, short-circuit GSX1 and AIN1N.

VFRO0 and VFRO1

These are receive analog output pins. VFRO0 and VFRO1 are connected to output pins of amplifiers AMP2 and AMP3. Output of output signals, VFRO0 and VFRO1, can be selected using the VFRO0 selection register (VFRO0_SEL) and VFRO1 selection register (VFRO1_SEL): When output is selected ("1"), the receive signal is output and when output is not selected ("0"), AVREF (about 1.4 V) is output. In power down mode, these output pins are set to a high impedance state. It is recommended to use output signals through a DC coupling capacitor.

(Note)

If output selection is changed while the conversation is in progress, a micronoise is generated. Therefore, it is recommended to select output before starting a call and then start a call.

Before canceling reset or resetting, it is recommended to select output of VFRO0 and VFRO1 to the AVREF output side.

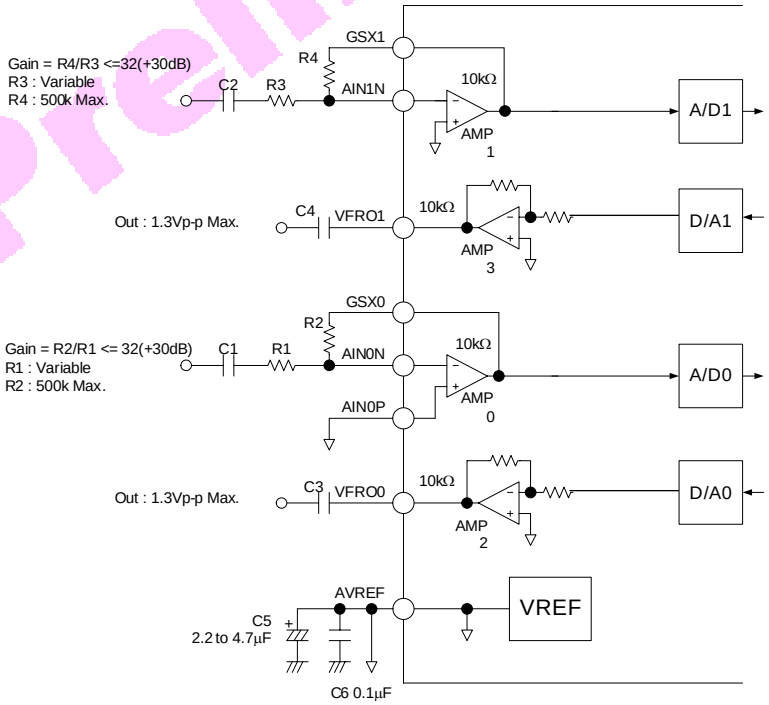


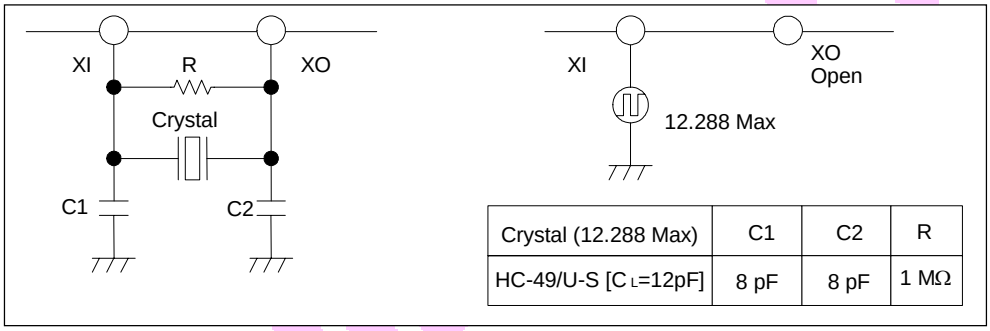
Figure 9 Analog Interface

AVREF

This is an output pin of an analog signal ground potential. With the output potential of about 1.4 V, insert bypass capacitors of 2.2 to 4.7 µF (aluminum electrolysis type) and 0.1 µF (ceramic type) in parallel. AVREF outputs 0.0 V at power down. AVREF starts being powered up after power-down reset, the system restarts from (PDNB = "1" and SPDN = "0"). Also, if the output from the AVREF pin will be used externally, use it via a buffer.

XI and XO

These are the master clock input pin (XI) and the crystal connection pins for the master clock (XI and XO). Oscillation stops at power down by PDNB or software power down by SPDN. Oscillation starts after power-down is reset and the clock is supplied to the LSI internal section after oscillation stabilization delay time has elapsed (about 21.3 ms). Figure 10 shows a master clock input example.



Crystal (12.288 Max)	C1	C2	R
HC-49/U-S [C_L=12pF]	8 pF	8 pF	1 MΩ

Figure 10 Example of an Oscillation Circuit and Clock Input

(Note)

For an oscillation circuit, connect a 12,288 MHz crystal and a 1 MΩ feedback resistor (R) between XI and XO. Since the values of capacitors C1 and C2 that are connected between XI and GND and between XO and GND are affected by the production load capacitance of a crystal and the wiring capacitance of the board, contact the manufacturer of the crystal to ask for matching evaluation to detemine the capacitor values.

CLKOUT

This is a 12.288 MHz master clock output pin.

Since output is disabled in the initial state, set the 12.288 MHz clock output enable control register (CLKOUT_EN) to "1" when clock output is required.

PDNB
This is a power-down control input pin. A power-down state can be set by setting this pin to "0". This pin also functions as an LSI reset pin. To prevent an LSI operation error, use PDNB for the initial power-down reset after power is applied. To put the LSI into a power-down state, fix PDNB to "0" for 250 μs or more.
LSI power-down reset can be performed by setting the software power down reset control register SPDN to "0" → "1" → "0".
Power-down is released, the initial mode display register (READY) is set to "1" after 200 ms, and various function setting modes (initial modes) are entered.
See Figure 1 for the timings of PDNB, AVREF, XO, and the initial mode.

(Note)
Turn on the power in a power-down state by PDNB.
When using the LSI by inputting a master clock to the XI pin, first maintain the power-down state (PDNB = 0) until power is applied to the digital power supply (DVD0, 1, and 2) and the analog power supply (AVDD) (90% or more) and the master clock is input to the XI pin, then release the power-down state (PDNB = 0 → 1) . In this case also, fix PDNB to "0" for 250 μs or more.

DVDD0, DVDD1, DVDD2, and AVDD
These are power supply pins. DVDD0, DVDD1, and DVDD2 are connected to the power supply of a digital circuit and AVDD is connected to a power supply of an analog circuit. Connect these pins near the LSI and insert bypass capacitors of 10 μF (electrolysis type) and 0.1 μF (ceramic type) between DGND and AGND in parallel.

DGND0, DGND1, DGND2, and AGND
These are ground pins. DGND0, DGND1, and DGND2 are connected to grounds of digital circuits and AGND is connected to a ground of an analog circuit. Connect these pins near the LSI.

VREGOUT
This is an output pin of an internal regulator voltage (about 2.5 V).
Connect a capacitor of about 0.1 μF (ceramic type) in parallel to about 10 μF (ceramic or tantalum type) between this pin and a ground pin.

VBG
This is a reference output pin for an internal regulator.
Connect a laminated ceramic capacitor of about 150 pF between this pin and a ground pin.

TST0, TST1, and TST2
These are input pins for testing. At normal use, input "0".

INTB/GPIOA[6]

Primary function: INTB

This is an interrupt request output pin as an extended function, but it is not supported in this code. If this pin is not used as the GPIOA[6] pin, which a secondary function is assigned to , leave it open.

(Caution) The INTB pin is assigned as an extended function; however, it is not supported in this code.
Note that although the INTB pin normally has "H" output, "L" may be output for about 15.6 µsec when DSP_ERR occurs.

Secondary function: GPIOA[6]

When the primary function/secondary function selection register (GPFA[6]) of GPIOA[6] is set to "1", this pin functions as a general-purpose I/O port GPIOA[6].

A0-A7

These are address input pins for accessing a frame/DMA/control register. Each address is as follows.

Transmit buffer (TX Buffer)
A7-A0 = 80h
Receive buffer (RX Buffer)
A7-A0 = 81h
Control register (CR)
See "A list of control registers" in the "CONTROL REGISTERS" Section for the addresses.

D0-D15

These are data I/O pins for accessing a frame/DMA/control register. Since these pins are I/O pins, connect pull-up resistors. When an 8-bit bus access is selected in the MCU interface data width selection register (BW_SEL), pins D0-D7 are enabled. When using the pins with 8-bit bus access (BW_SEL = "1"), fix the input of high-order D8-D15 to either "0" or "1" since they are constantly in an input state.

CSB

This is a chip select input pin for accessing a frame/control register.

RDB

This is a read enable input pin for accessing a frame/DMA/control register.

WRB

This is a write enable input pin for accessing a frame/DMA/control register.

FR0B (DMARQ0B)

- FR0B (FRAME/DMA selection register FD_SEL = "0" in frame mode)
  This is a transmit frame output pin that outputs data when the transmit buffer for frame access becomes full. When the transmit buffer becomes full, the pin outputs "L" and retains "L" until the specified number of words are read from the MCU.

- DMARQ0B (FRAME/DMA selection register FD_SEL = "1" in DMA mode)
  This is a DMA request output pin that outputs data when the transmit buffer for DMA access becomes full. When the transmit buffer becomes full, the pin outputs "L" and the value is reset to "H" automatically when an acknowledgment signal (ACK0B = "0") and the fall of a read enable signal (RDB = "1" → "0") are received from the MCU side. This operation is repeated until the specified number of words are read from the MCU.

FR1B (DMARQ1B)

- FR1B (FRAME/DMA selection register FD_SEL = "0" in frame mode)
  This receive frame output pin outputs data when the receive buffer for frame access becomes empty. When the receive buffer becomes empty, the pin outputs "L" and retains "L" until the specified number of words are written from the MCU.

- DMARQ1B (FRAME/DMA selection register FD_SEL = "1" in DMA mode)
  This a DMA request output pin that outputs data when the receive buffer for DMA access becomes empty. When the receive buffer becomes empty, the pin outputs "L" and the value is reset to "H" automatically when an acknowledgment signal (ACK1B = "0") and the fall of a write enable signal (WRB = "1" → "0") are received from the MCU side. This opeation is repeated until the specified number of words are written from the MCU side.

ACK0B/GPIOA[4]

Primary function: ACK0B

This is a DMA acknowledgment input pin for DMARQ0B for transmit buffer DMA access; it is enabled in DMA mode (FD_SEL = "1").
When using the pin in frame mode (FD_SEL = "0"), fix this pin to "1".

Secondary function: GPIOA[4]

When the primary function/secondary function selection register (GPFA[4]) of GPIOA[4] is set to "1", the pin functions as a general-purpose I/O port GPIOA[4].

ACK1B/GPIOA[5]

Primary function: ACK0B

This is a DMA acknowledgment input pin for DMARQ1B for receive buffer DMA access; it is enabled in DMA mode (FD_SEL = "1").
When using this pin in frame mode (FD_SEL = "0"), fix this pin to "1".

Secondary function: GPIOA[5]

When the primary function/secondary function selection register (GPFA[5]) of GPIOA[5] is set to "1", the pin functions as a general-purpose I/O port GPIOA[5].

GPIOA[0], GPIOA[1], GPIOA[2], and GPIOA[3]

These are general-purpose I/O ports A[3:0].
However, the following secondary functions are assigned to GPIOA[2].
Secondary function of GPIOA[2]: Output pin (DPO) of the dual pulse transmitter (DPGEN)
Also, GPIOA[0] and GPIOA[1] are used as the input pins of the dial pulse detector as shown below.
GPIOA[0]: Input pin (DP0) of a dial pulse detector (DPDET0)
GPIOA[1]: Output pin (DP1) of a dial pulse detector (DPDET1)

GPIOB[5:0]
This is a general-purpose I/O port B[5:0].

GPIOC[7:0]
This is a general-purpose I/O port C[7:0].

CLKSEL
This is an input-output control input pin of SYNC and BCLK. The pin controls input when it is set to "0" and output when it is set to "1".
(Note)
This LSI operates at either SYNC/BCLK that is generated inside the LSI or the clock generated based on SYNC/BCLK to be input from the outside the LSI. For this reason, if the CLKSEL pin is set to "0", it is necessary to constantly input SYNC/BCLK from the time the power supply is truned on regardless of whether PCM-IF is used or not.

SYNC
This is a 8 kHz synchronous signal I/O pin of PCM signals. When CLKSEL is "0", constantly input an 8 kHz clock synchronized with BCLK. When CLKSEL is "1", this pin outputs an 8 kHz clock synchronized with BCLK. When the SYNC frame control register (SYNC_SEL) is "0", long frame synchronization is specified and when the register is "1", short frame synchronization is specified.

BCLK
This is a shift clock I/O pin of a PCM signal.
When CLKSEL is "0", clock input synchronized with SYNC is necessary. Always input a clock of 128kHz to 2.048MHz after turning on the power. When CLKSEL is "1", this pin outputs a clock of 2.048 MHz synchronized with SYNC.

(Remarks) Table 1 shows the input-output control of SYNC and BCLK and the frequencies.

Table 1 SYNC and BCLK Input-Output Control

CLKSEL	SYNC	BCLK	Remarks
"0"	Input (8 kHz)	Input (128 kHz to 2048 kHz)	Always input a clock of 128 kHz to 2.048 MHz after start of power supply.
"1"	Output (8 kHz)	Output (2.048 MHz)	At power down, "L" is output.

PCMO
This is a PCM signal output pin. A PCM signal is output synchronized with the rise of BCLK or SYNC.
For the output from PCMO, data is output to only the applicable time slot section according to the selected coding format and the setting of the time slot position and other sections are set to a high-impedance state. If a PCM interface is not used, PCMO is set to a high impedance state.

(Note)
Be sure to connect a pull-up resistor externally to the PCMO pin, because the pin is an open drain output pin.
Do not use a pull-up voltage greater than the digital power supply voltage (DVDD).

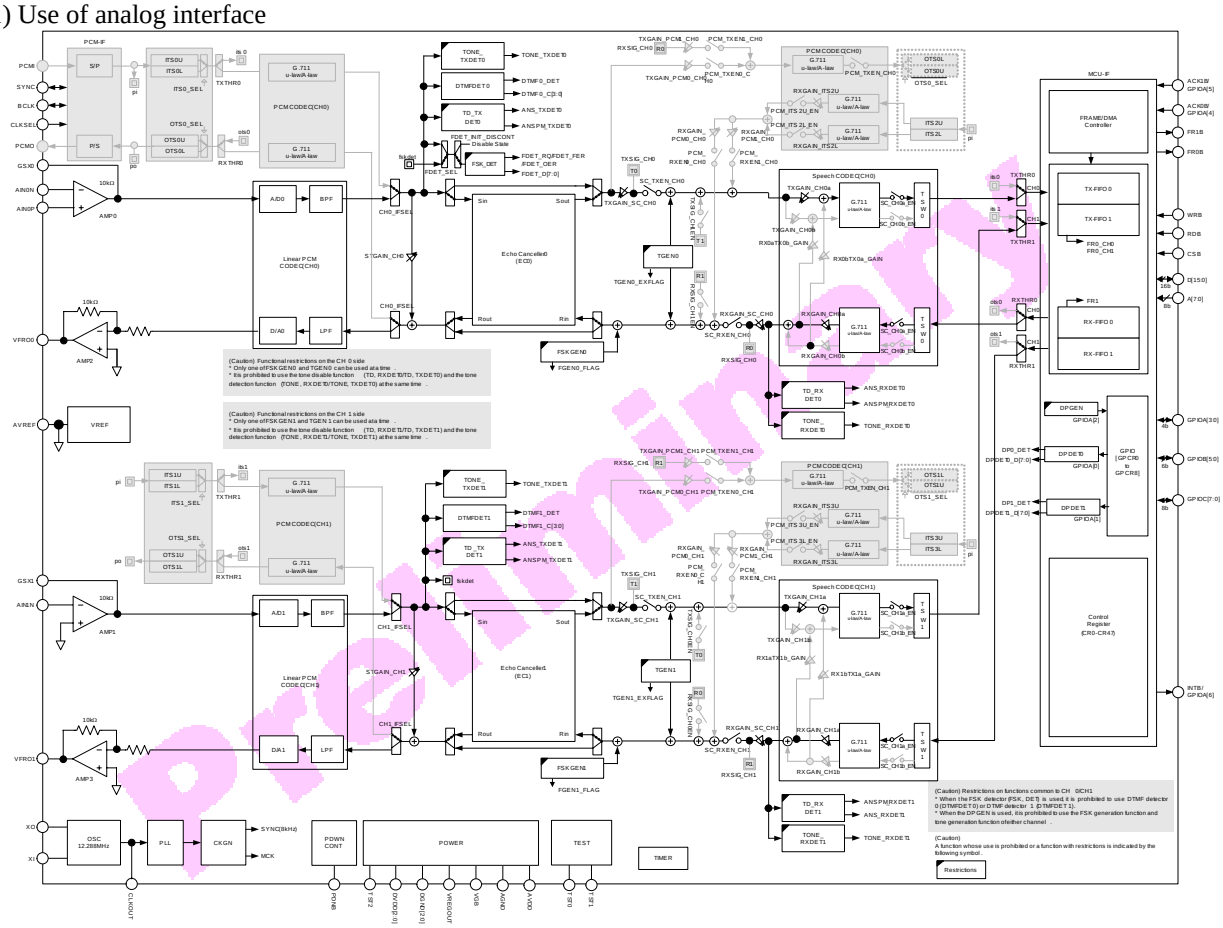
PCMI
This is a PCM signal input pin. The signal is shifted at falling of BCLK and is input from MSB.
If a PCM interface is not used, fix the input to "0" or "1".

APPLICATION CONFIGURATION EXAMPLES

Configuration Example 1 (Basic Speech)

This configuration example shows when speech is performed between an analog phone (A-TEL) connected to the terminal side and the network side.

(1) Use of analog interface



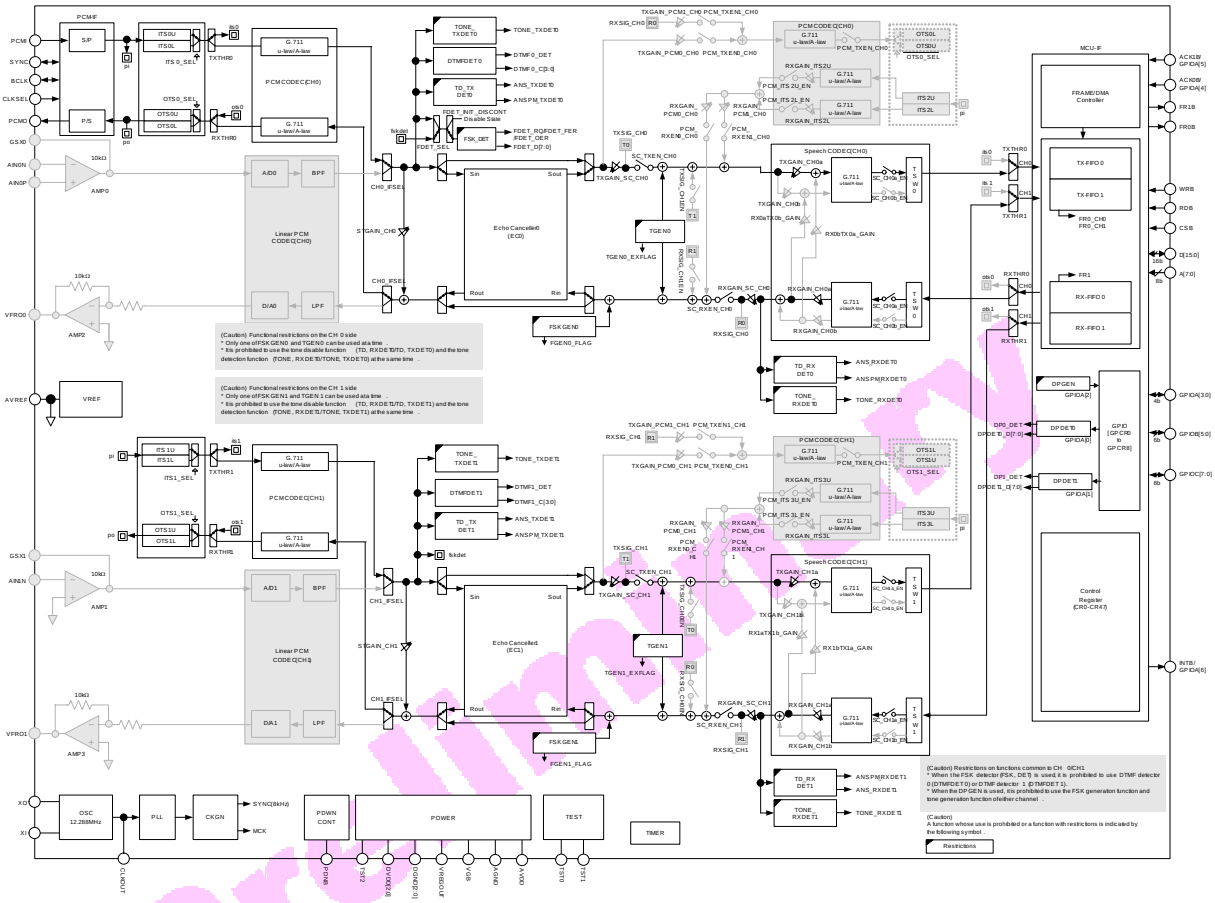
Setting Examples

- CR10=06h (CH0/CH1 terminal interface: Analog interface, VFRO0/VFRO1=Voice output)
- CR13=12h (Frame/16B/G.711 μ-law/10msec)
- Speech path switch setting
- CR6=03h, CR7=8Bh, CR8=00h, CR9=08h, CR1=80h (Address: 038Bh Data: 0008h)

* When the decoded output start offset time is 1 msec

- CR24=04h (G711_PLCEN="1")
- Various settings
- CR0=01h (LONG/OPE_STAT="1")
- CR24=ACh (SC_CH0aEN=SC_CH1aEN=DEC_OUTON=G711_PLCEN="1")

(2) Use of PCM interface



Setting Examples

- CR10=C0h (CH0/CH1 terminal interface: PCM I/F, VFRO0/VFRO1=AVREF)
- CR13=12h (Frame/16B/G.711 μ-law/10msec)
- Speech path switch setting
- CR6=03h, CR7=8Bh, CR8=00h, CR9=08h, CR1=80h (Address: 038Bh Data:0008h)

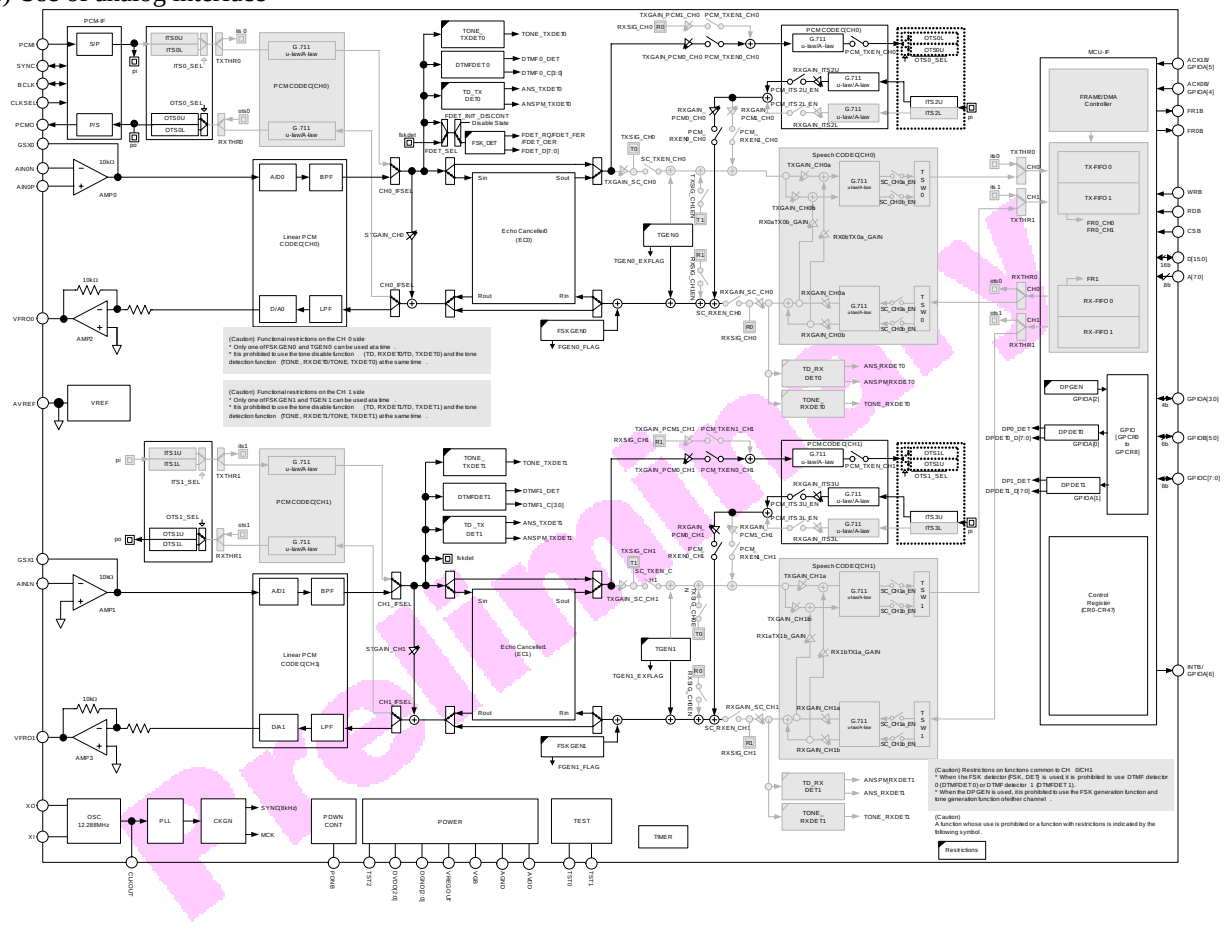
* When the decoded output start offset time is 1 msec

- CR14=40h (G.711 μ-law)
- CR24=04h (G711_PLCEN="1")
- CR33=xxh, CR34=xxh, CR35=xxh, CR38=xxh (ITS0, ITS1, OTS0, OTS1 slot specification)
- Various settings
- CR0=61h (AFE0_PDN=AFE1_PDN=LONG/OPE_STAT="1")
- CR11=0Fh (PCMI0_EN=PCMI1_EN=PCMO0_EN=PCMO1_EN="1")
- CR24=ACh (SC_CH0aEN=SC_CH1aEN=DEC_OUTON=G711_PLCEN="1")

Configuration Example 2 (Speech Using Extension with PCM)

This configuration example shows when an extension speech is made between analog phones (A-TEL1, A-TEL2) with a unit that has two ports of analog phone interface.

(1) Use of analog interface



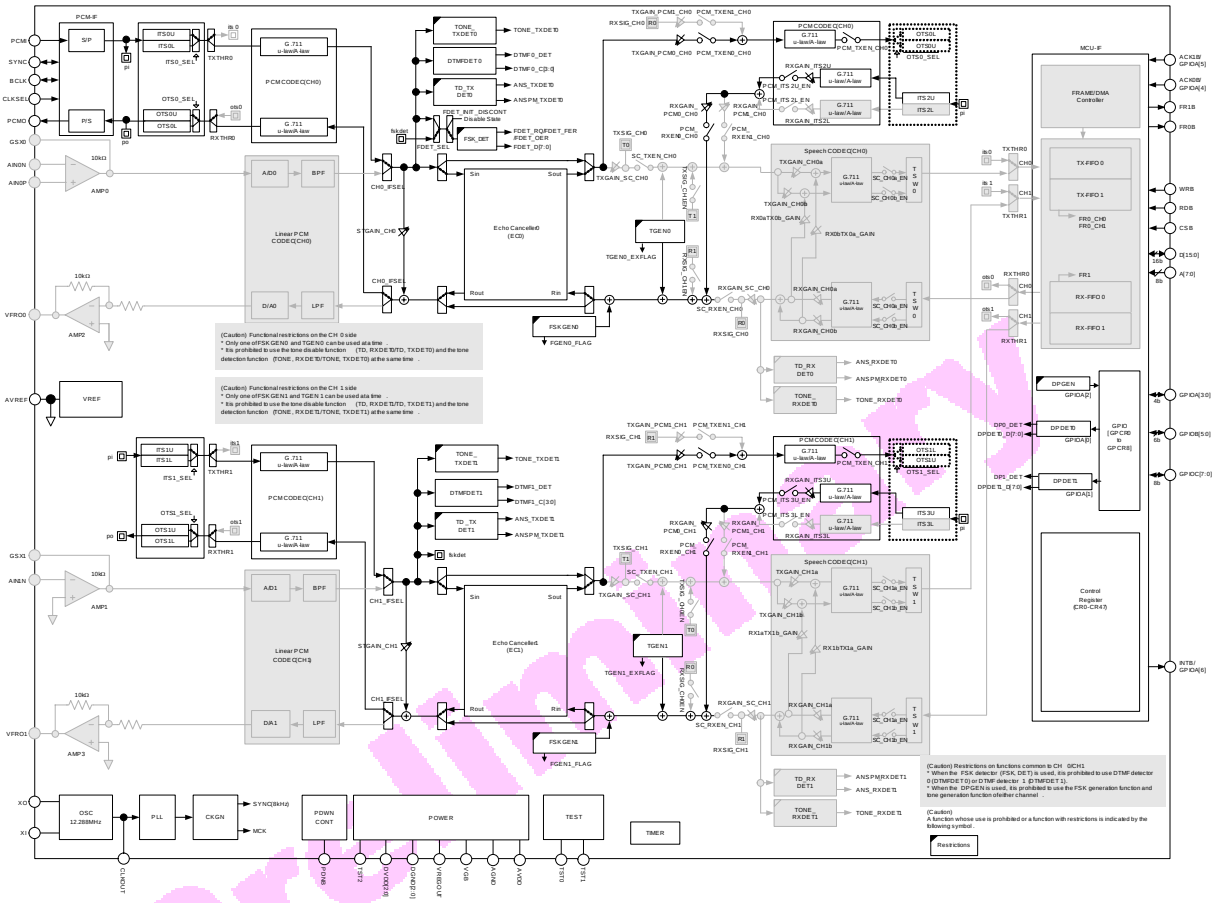
Setting Examples

- CR10=06h (CH0/CH1 terminal interface: Analog interface, VFRO0/VFRO1=Voice output)
- Speech path switch setting
- CR14=40h (G.711 μ-law)
- CR35=xxh, CR36=xxh, CR37=xxh, CR38=xxh (ITS2, ITS3, OTS0, OTS1 slot specification)
- Various settings
- CR0=01h (LONG/OPE_STAT="1")
- CR11=39h (PCMI2_EN=PCMI3_EN=PCMO0_EN=PCMO1_EN="1")

(Note)

The time slot position where PCM data is output when an extension speech and so forth is made via the PCM interface will be the opposite side of the upper 8 bits or lower 8 bits selected by CR35-B7 (OTS0_SEL) or CR38-BIT7(OTS1_SEL). Please be careful as this also applies to configuration examples 3, 4 and 6.

(2) Use of PCM interface



Setting Examples

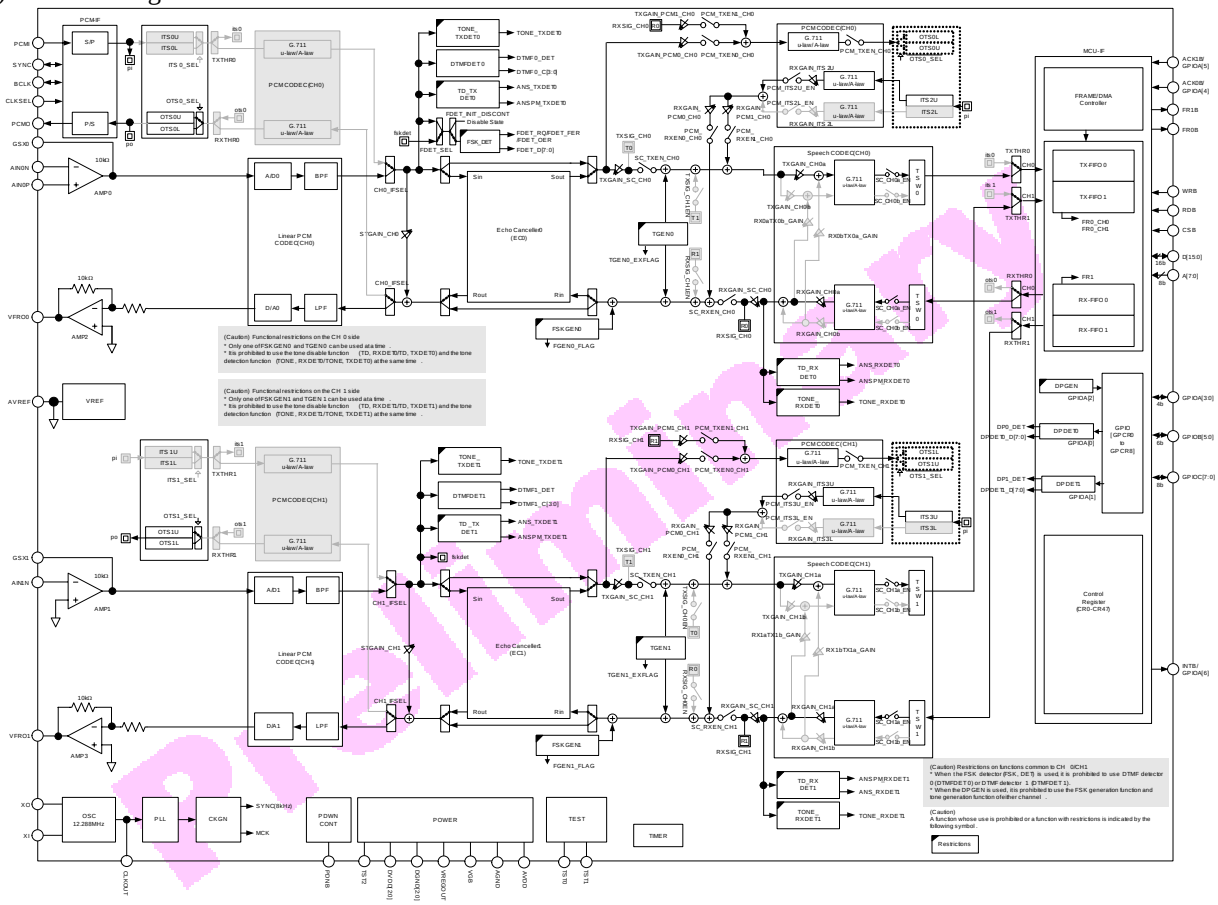
- CR10=C0h (CH0/CH1 terminal interface: PCM I/F, VFRO0/VFRO1=AVREF)
- Speech path switch setting
- CR14=40h (G.711 μ-law)
- CR33=xxh, CR34=xxh, CR35=xxh, CR36=xxh, CR37=xxh, CR38=xxh
  (ITS0, ITS1, ITS2, ITS3, OTS0, OTS1 slot specification)
- Various settings
- CR0=61h (AFE0_PDN=AFE1_PDN=LONG/OPE_STAT="1")
- CR11=3Fh (PCMI0_EN=PCMI1_EN=PCMI2_EN=PCMI3_EN=PCMO0_EN=PCMO1_EN="1")

(Note)

The time slot position where PCM data is output when an extension speech and so forth is made via the PCM interface will be the opposite side of the upper 8 bits or lower 8 bits selected by CR35-B7 (OTS0_SEL) or CR38-BIT7(OTS1_SEL). The slot position where the PCM data to the terminal side is output will be the upper 8 bits or lower 8 bits selected by CR35-B7(OTS0_SEL) or CR38-BIT7(OTS1_SEL). Please be careful as this also applies to configuration examples 3, 4 and 6.

Configuration Example 3 (Three-Way Speech: Terminal Side [Two Parties] – NW Side [One Party])
This configuration example shows when three-way speech is performed among an analog phone (A-TEL1) connected to the terminal side of this LSI, an analog phone (A-TEL2) connected to other device on the PCM interface, and the network side (one party).

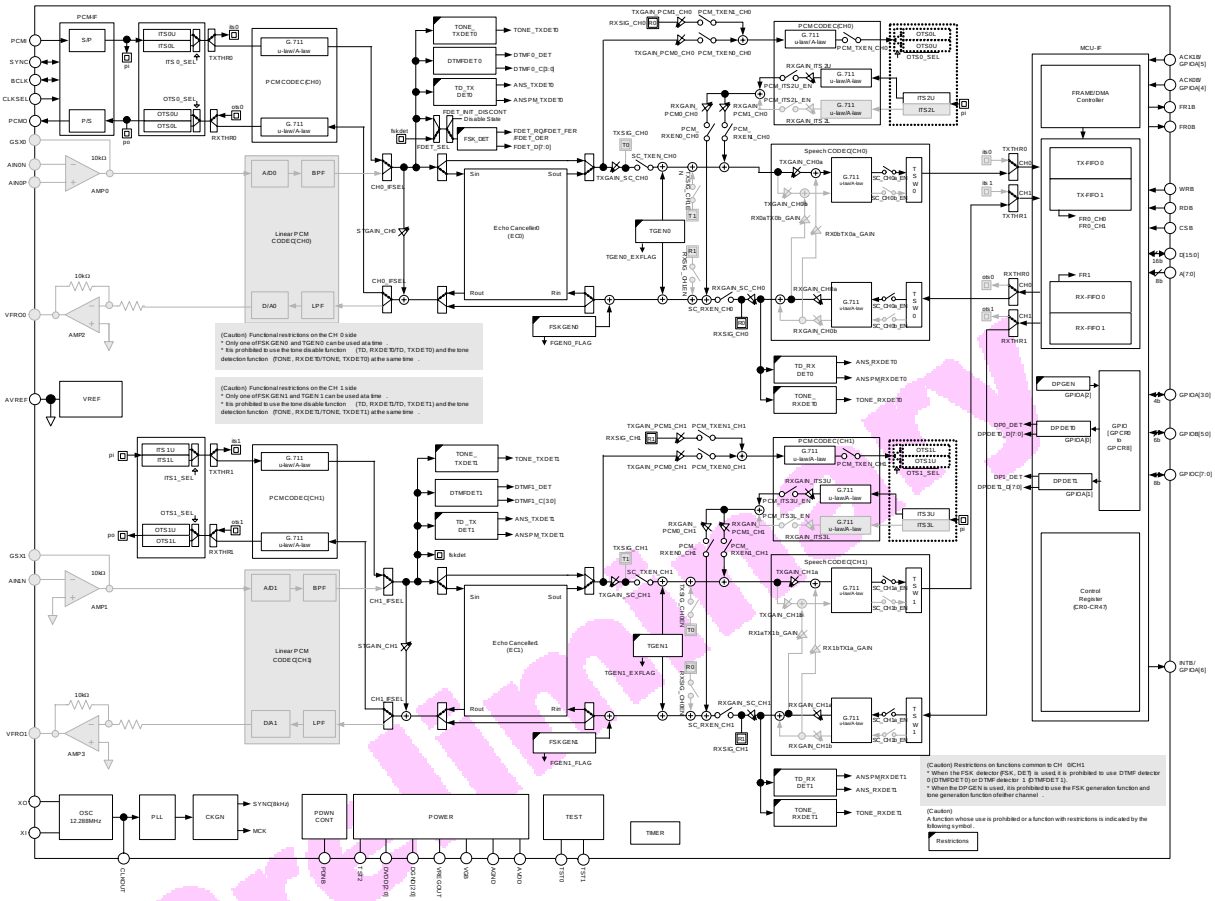
(1) Use of analog interface



Setting Examples
- CR10=06h (CH0/CH1 terminal interface: Analog interface, VFRO0/VFRO1=Voice output)
- CR13=12h (Frame/16B/G.711 μ-law/10msec)
- Speech path switch setting
- CR6=03h, CR7=8Bh, CR8=00h, CR9=08h, CR1=80h (Address: 038Bh Data: 0008h)

* When the decode output start offset time is 1 msec
- CR14=40h (G.711 μ-law)
- CR24=04h (G711_PLCEN="1")
- CR35=xxh, CR36=xxh, CR37=xxh, CR38=xxh (ITS2, ITS3, OTS0, OTS1 slot specification)
- Various settings
- CR0=01h (LONG/OPE_STAT="1")
- CR11=39h (PCMI2_EN=PCMI3_EN=PCMO0_EN=PCMO1_EN="1")
- CR24=ACh (SC_CH0aEN=SC_CH1aEN=DEC_OUTON=G711_PLCEN="1")

(2) Use of PCM interface



Setting Examples

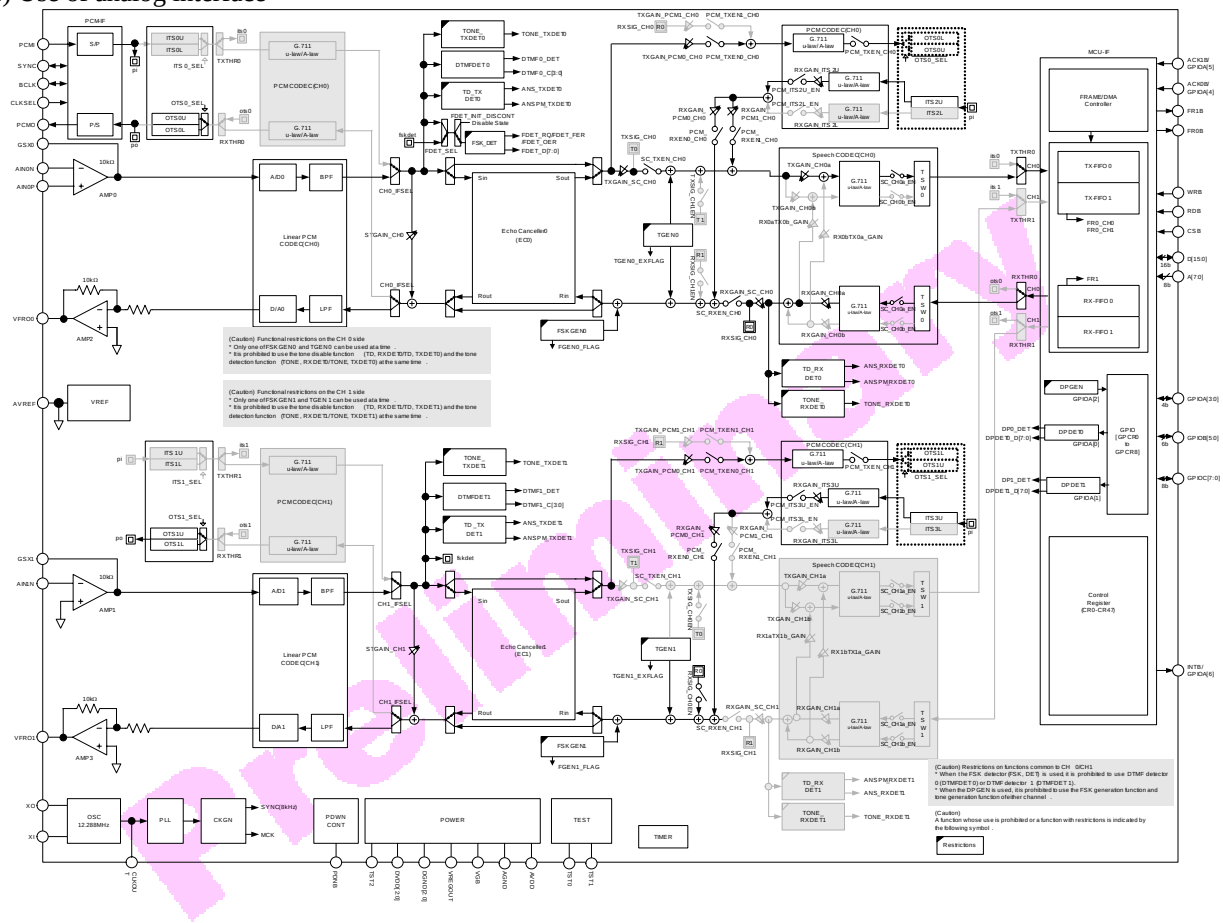
- CR10=C0h (CH0/CH1 terminal interface: PCM I/F, VFRO0/VFRO1=AVREF)
- CR13=12h (Frame/16B/G.711 μ-law/10msec)
- Speech path switch setting
- CR6=03h, CR7=8Bh, CR8=00h, CR9=08h, CR1=80h (Address: 038Bh Data: 0008h)

* When the decode output start offset time is 1 msec

- CR14=40h (G.711 μ-law)
- CR24=04h (G711_PLCEN="1")
- CR33=xxh, CR34=xxh, CR35=xxh, CR36=xxh, CR37=xxh, CR38=xxh
  (ITS0, ITS1, ITS2, ITS3, OTS0, OTS1 slot specification)
- Various settings
- CR0=61h(AFE0_PDN=AFE1_PDN=LONG/OPE_STAT="1")
- CR11=3Fh(PCMI0_EN=PCMI1_EN=PCMI2_EN=PCMI3_EN=PCMO0_EN=PCMO1_EN="1")
- CR24=ACh(SC_CH0aEN=SC_CH1aEN=DEC_OUTON=G711_PLCEN="1")

Configuration Example 4 (Three-Way Speech: Terminal Side [Two Parties] – NW Side [One Party])
This configuration example shows when three-way speech is performed among an analog phone (A-TEL1) connected to CH0, an analog phone (A-TEL2) connected to CH1, and the network side (one perty).

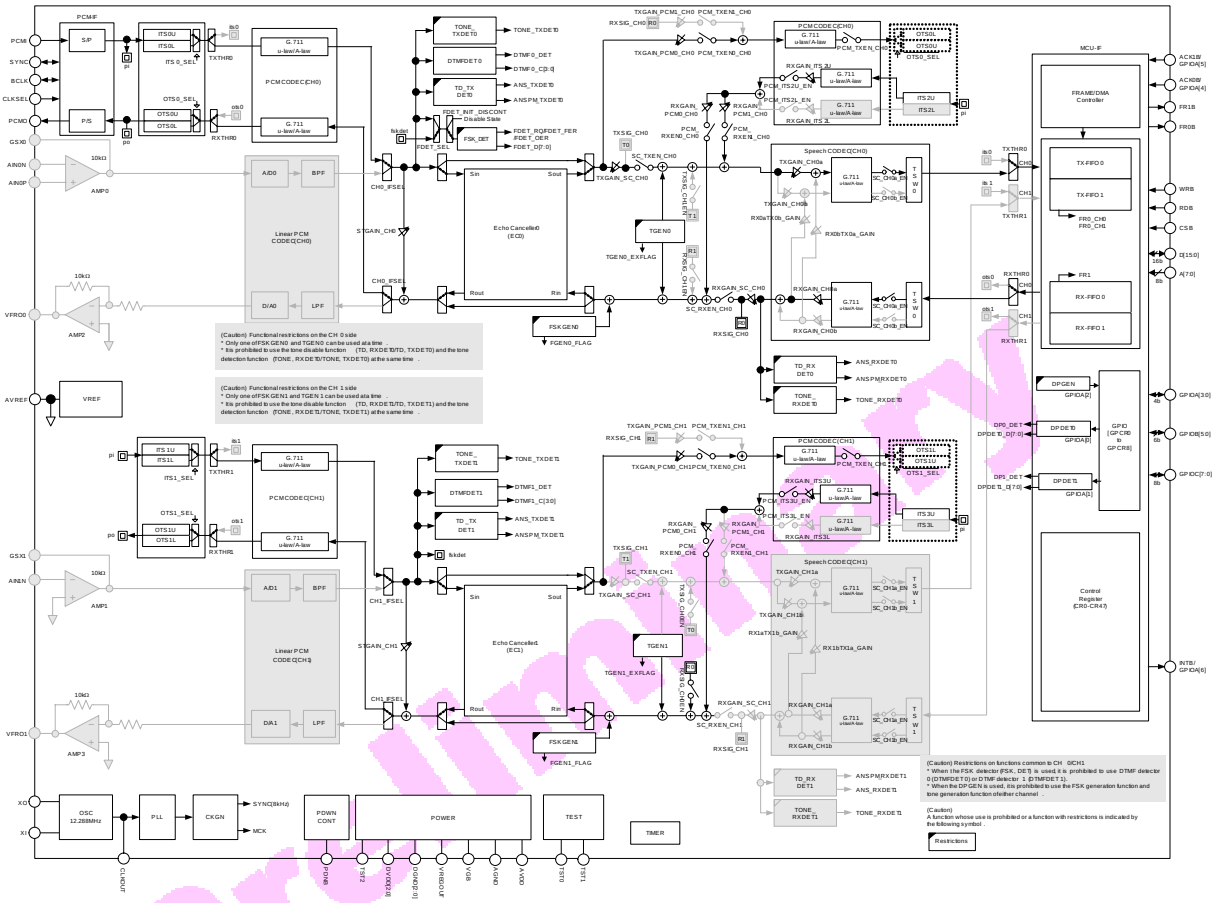
(1) Use of analog interface



Setting Examples
- CR10=06h (CH0/CH1 terminal interface: Analog interface, VFRO0/VFRO1=Voice output)
- CR13=12h (Frame/16B/G.711 μ-law/10msec)
- Speech path switch setting
- CR6=03h, CR7=8Bh, CR8=00h, CR9=08h, CR1=80h (Address: 038Bh Data: 0008h)

* When the decode output start offset time is 1 msec
- CR14=40h (G.711 u-law)
- CR24=04h (G711_PLCEN="1")
- CR35=xxh, CR36=xxh, CR37=xxh, CR38=xxh (ITS2, ITS3, OTS0, OTS1 slot specification)
- Various settings
- CR0=01h (LONG/OPE_STAT="1")
- CR11=39h (PCMI2_EN=PCMI3_EN=PCMO0_EN=PCMO1_EN="1")
- CR24=8Ch (SC_CH0aEN=DEC_OUTON=G711_PLCEN="1")

(2) Use of PCM interface



Setting Examples

- CR10=C0h (CH0/CH1 terminal interface: PCM I/F, VFRO0/VFRO1=AVREF)
- CR13=12h (Frame/16B/G.711 μ-law/10msec)
- Speech path switch setting
- CR6=03h, CR7=8Bh, CR8=00h, CR9=08h, CR1=80h (Address: 038Bh Data: 0008h)

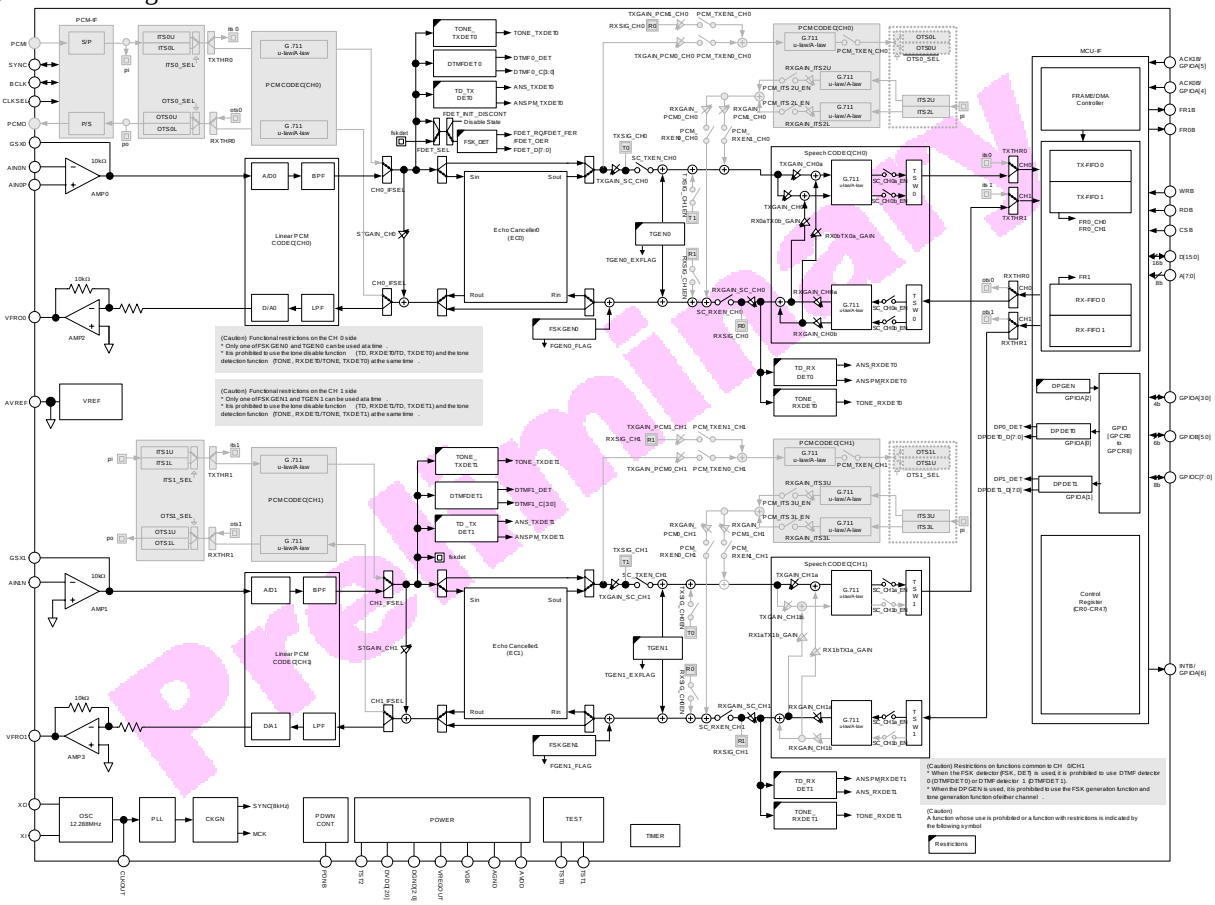
* When the decode output start offset time is 1 msec

- CR14=40h (G.711 μ-law)
- CR24=04h (G711_PLCEN="1")
- CR33=xxh, CR34=xxh, CR35=xxh, CR36=xxh, CR37=xxh, CR38=xxh
  (ITS0, ITS1, ITS2, ITS3, OTS0, OTS1 slot specification)
- Various settings
- CR0=61h (AFE0_PDN=AFE1_PDN=LONG/OPE_STAT="1")
- CR11=3Fh (PCMI0_EN=PCMI1_EN=PCMI2_EN=PCMI3_EN=PCMO0_EN=PCMO1_EN="1")
- CR24=8Ch (SC_CH0aEN=DEC_OUTON=G711_PLCEN="1")

Configuration Example 5 (Three-Way Speech: Terminal Side [One Party] – NW Side [Two Parties])

This configuration example shows when three-way speech is performed among an analog phone (A-TEL) connected to the terminal side and the network side (two parties).
Please be aware that three-way speech cannot be performed among the terminal side (one party) and the network side (two parties) between CH0 and CH1. In this configuration example, the CH1 side shows when the basic speech is performed.

(1) Use of analog interface



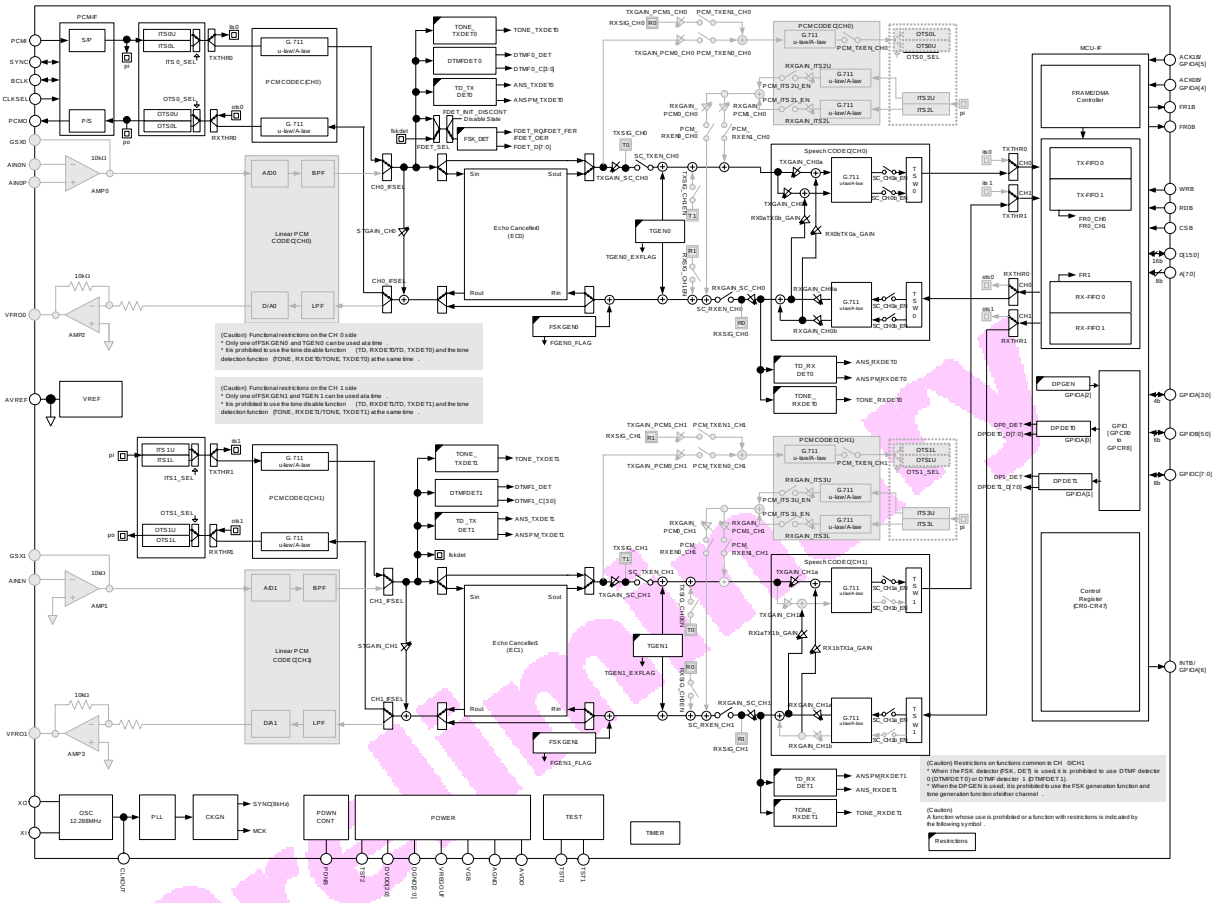
Setting Examples

- CR10=06h (CH0/CH1 terminal interface: Analog interface, VFRO0/VFRO1=Voice output)
- CR13=12h (Frame/16B/G.711 μ-law/10msec)
- CR6=03h, CR7=8Bh, CR8=00h, CR9=08h, CR1=80h (Address: 038Bh Data: 0008h)

* When the decode output start offset time is 1 msec

- CR24=04h (G711_PLCEN="1")
- Various settings
- CR0=01h (LONG/OPE_STAT="1")
- CR24=ECh (SC_CH0aEN=SC_CH0bEN=SC_CH1aEN=DEC_OUTON=G711_PLCEN="1")

(2) Use of PCM interface



Setting Examples

- CR10=C0h (CH0/CH1 terminal interface: PCM I/F, VFRO0/VFRO1=AVREF)
- CR13=12h (Frame/16B/G.711 μ-law/10msec)
- Speech path switch setting
- CR6=03h, CR7=8Bh, CR8=00h ,CR9=08h, CR1=80h (Address: 038Bh Data: 0008h)

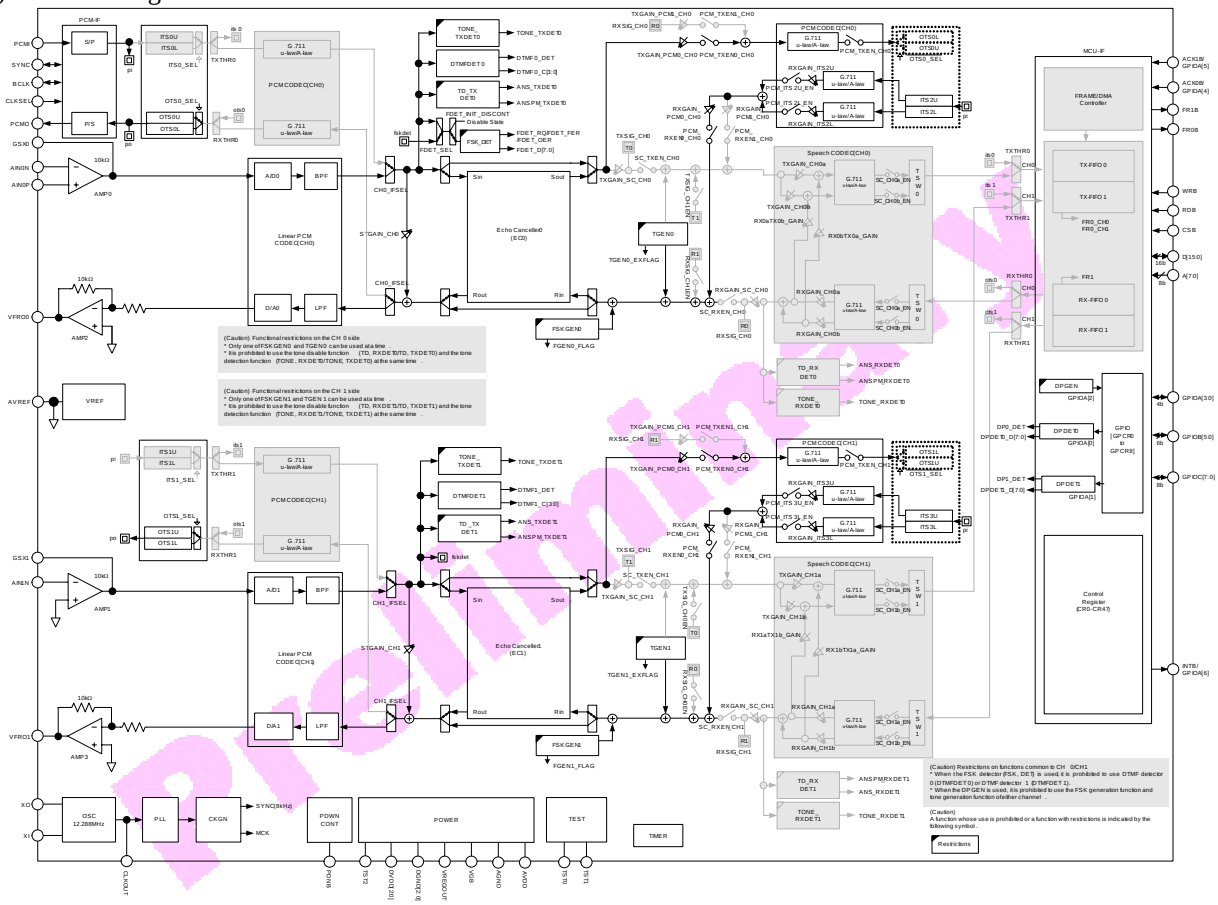
* When the decode output start offset time is 1 msec

- CR14=40h (G.711 μ-law)
- CR24=04h (G711_PLCEN="1")
- CR33=xxh, CR34=xxh, CR35=xxh, CR38=xxh (ITS0, ITS1, OTS0, OTS1 slot specification)
- Various settings
- CR0=61h (AFE0_PDN=AFE1_PDN=LONG/OPE_STAT="1")
- CR11=0Fh (PCMI0_EN=PCMI1_EN=PCMO0_EN=PCMO1_EN="1")
- CR24=ECh (SC_CH0aEN=SC_CH0bEN=SC_CH1aEN=DEC_OUTON=G711_PLCEN="1")

Configuration Example 6 (Three-Way Speech: Terminal Side [Three Parties])

This configuration example shows when three-way speech is performed among an analog phone (A-TEL1) connected to the terminal side of this LSI and analog phones (A-TEL2, A-TEL3) connected to other device on the PCM interface.

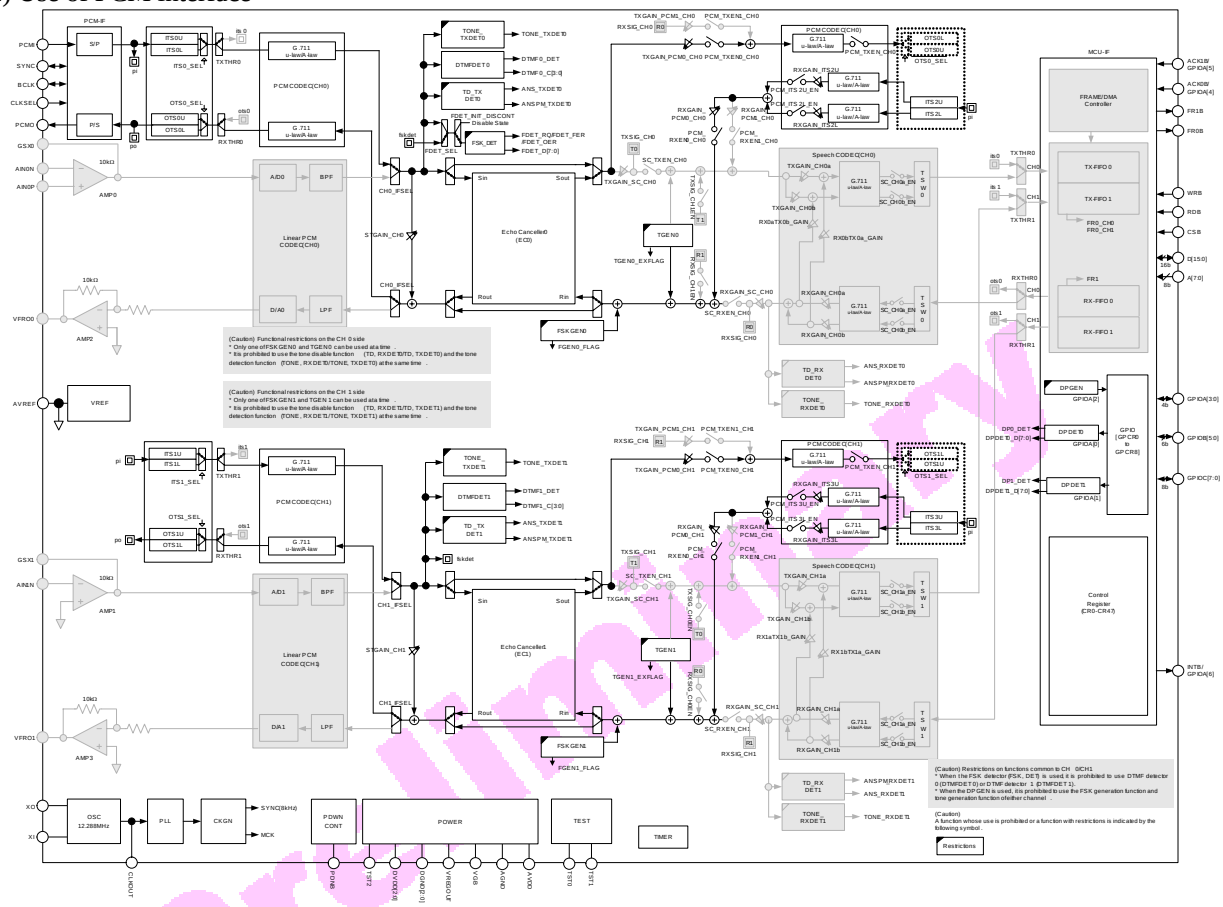
(1) Use of analog interface



Setting Examples

- CR10=06h (CH0/CH1 terminal interface: Analog interface, VFRO0/VFRO1=Voice output)
- Speech path switch setting
- CR14=40h (G.711 μ-law)
- CR35=xxh, CR36=xxh, CR37=xxh, CR38=xxh (ITS2, ITS3, OTS0, OTS1 slot specification)
- Various settings
- CR0=01h (LONG/OPE_STAT="1")
- CR11=39h (PCMI2_EN=PCMI3_EN=PCMO0_EN=PCMO1_EN="1")

(2) Use of PCM interface

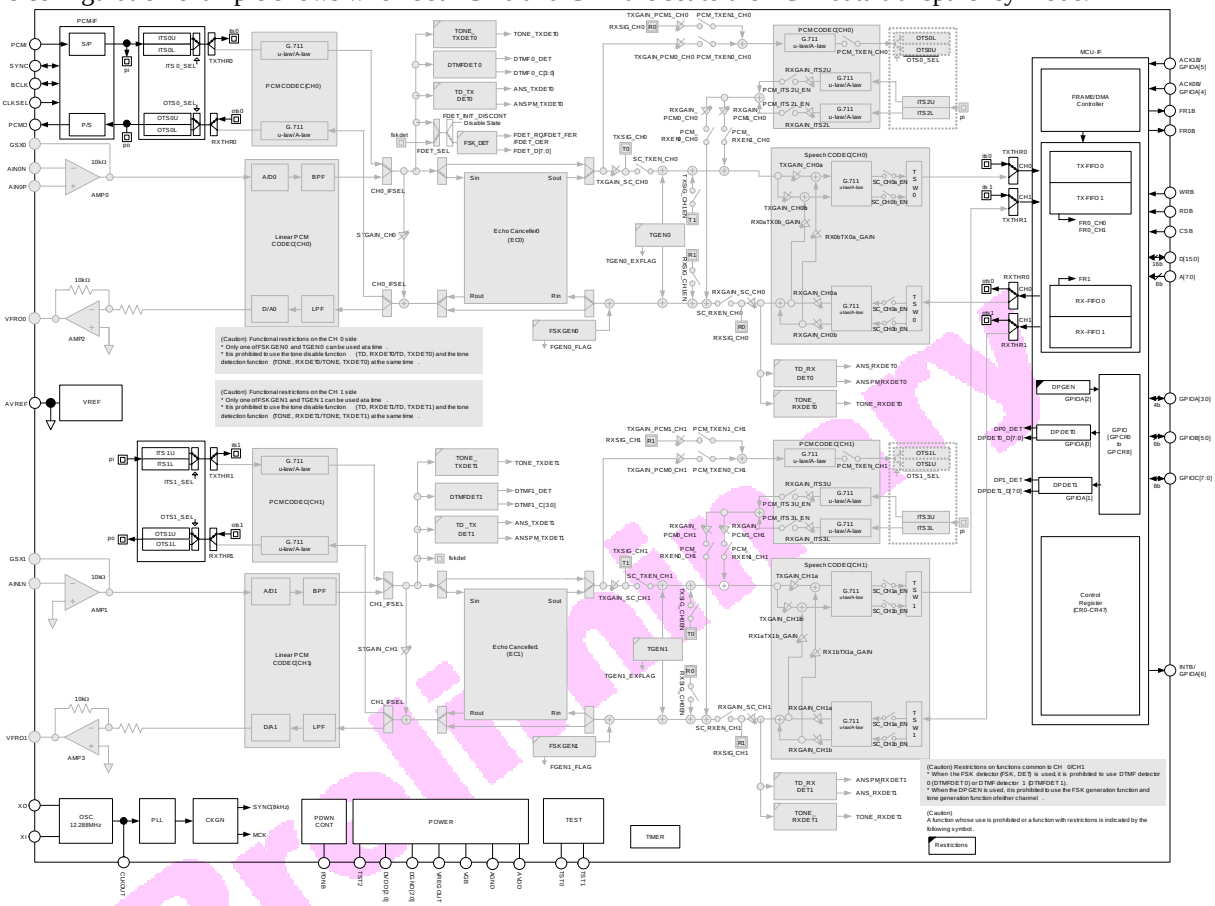


Setting Examples

- CR10=C0h (CH0/CH1 terminal interface: PCM I/F, VFRO0/VFRO1=AVREF)
- Speech path switch setting
- CR14=40h (G.711 μ-law)
- CR33=xxh, CR34=xxh, CR35=xxh, CR36=xxh, CR37=xxh, CR38=xxh
  (ITS0, ITS1, ITS2, ITS3, OTS0, OTS1 slot specification)
- Various settings
- CR0=61h (AFE0_PDN=AFE1_PDN=LONG/OPE_STAT="1")
- CR11=3Fh (PCMI0_EN=PCMI1_EN=PCMI2_EN=PCMI3_EN=PCMO0_EN=PCMO1_EN="1")

Configuration Example 7 (PCM Transparency Mode)

This configuration example shows when both CH0 and CH1 are set to the PCM data transparency mode.



Setting Examples

- CR10=C0h (CH0/CH1 terminal interface: PCM I/F, VFRO0/VFRO1=AVREF)
- CR13=12h (Frame/16B/G.711 μ-law/10msec)
- CR6=03h, CR7=8Bh, CR8=00h, CR9=08h, CR1=80h (Address: 038Bh Data: 0008h)

* When the decode output start offset time is 1 msec

- CR14=4Fh (G.711 μ-law /TXTHR0=TXTHR1=RXTHR0=RXTHR1="1")
- CR33=xxh, CR34=xxh, CR35=xxh, CR38=xxh (ITS0, ITS1, OTS0, OTS1 slot specification)
- CR0=61h (AFE0_PDN=AFE1_PDN=LONG/OPE_STAT="1")
- CR11=0Fh (PCMI0_EN=PCMI1_EN=PCMO0_EN=PCMO1_EN="1")
- CR24=A8h (SC_CH0aEN=SC_CH1aEN=DEC_OUTON="1")

NOTES ON USE

1. Only one of the FSK generation function and tone generation function (DTMF generation function) can be used at the same time in each channel.
   Exercise caution as the simultaneous use of two generation functions is prohibited. Also, if the dial pulse send function is used, it is prohibited to use the FSK generation function and tone generation function in one of the channels. For start control corresponding to each function described above, see the following table.

	CH0	CH1
Startup of FSK generation function	FGEN0_EN=1 (CR25-B5)	FGEN1_EN=1 (CR26-B5)
Startup of tone generation function	CR2=xxh (Other than 00h: Dependent on output tone)	CR3=xxh (Other than 00h: Dependent on output tone)
Startup of dial pulse transmit function	DPGEN_EN=1 (CR27-B6)	

2. It is prohibited to use the 2100 Hz single tone/phase inversion detection function and the tone detection function at the same time in each channel.
   Exercise caution as the simultaneous use of two generation functions is prohibited. For start control corresponding to each function described above, see the following table.

	CH0	CH1
Startup of 2100 Hz single tone/phase inversion detection function	TD_TXDET0EN=1 (CR25-B3) TD_RXDET0EN=1 (CR25-B4)	TD_TXDET1EN=1 (CR26-B3) TD_RXDET1EN=1 (CR26-B4)
Startup of tone generation function	TONE_TXDET0EN=1 (CR25-B6) TONE_RXDET0EN=1 (CR25-B7)	TONE_TXDET1EN=1 (CR26-B6) TONE_RXDET1EN=1 (CR26-B7)

3. When the FSK detection function is used, it is prohibited to use the DTMF detection function of either channel. For start control corresponding to each function described above, see the following table.

	CH0	CH1
Startup of FSK detection function	FDET_EN=1 (CR45-B4)	
Startup of DTMF detection function	DTMF0_EN (CR25-B2)	DTMF1_EN (CR26-B2)

4. The initial value of the PCM-IF coding format selection control register (PCM_SEL[1:0]) is [0:0]. To use PCM-IF, be sure to set [0:1] (G.711 u-law) or [1:1] (G.711 A-law) during the initial mode.

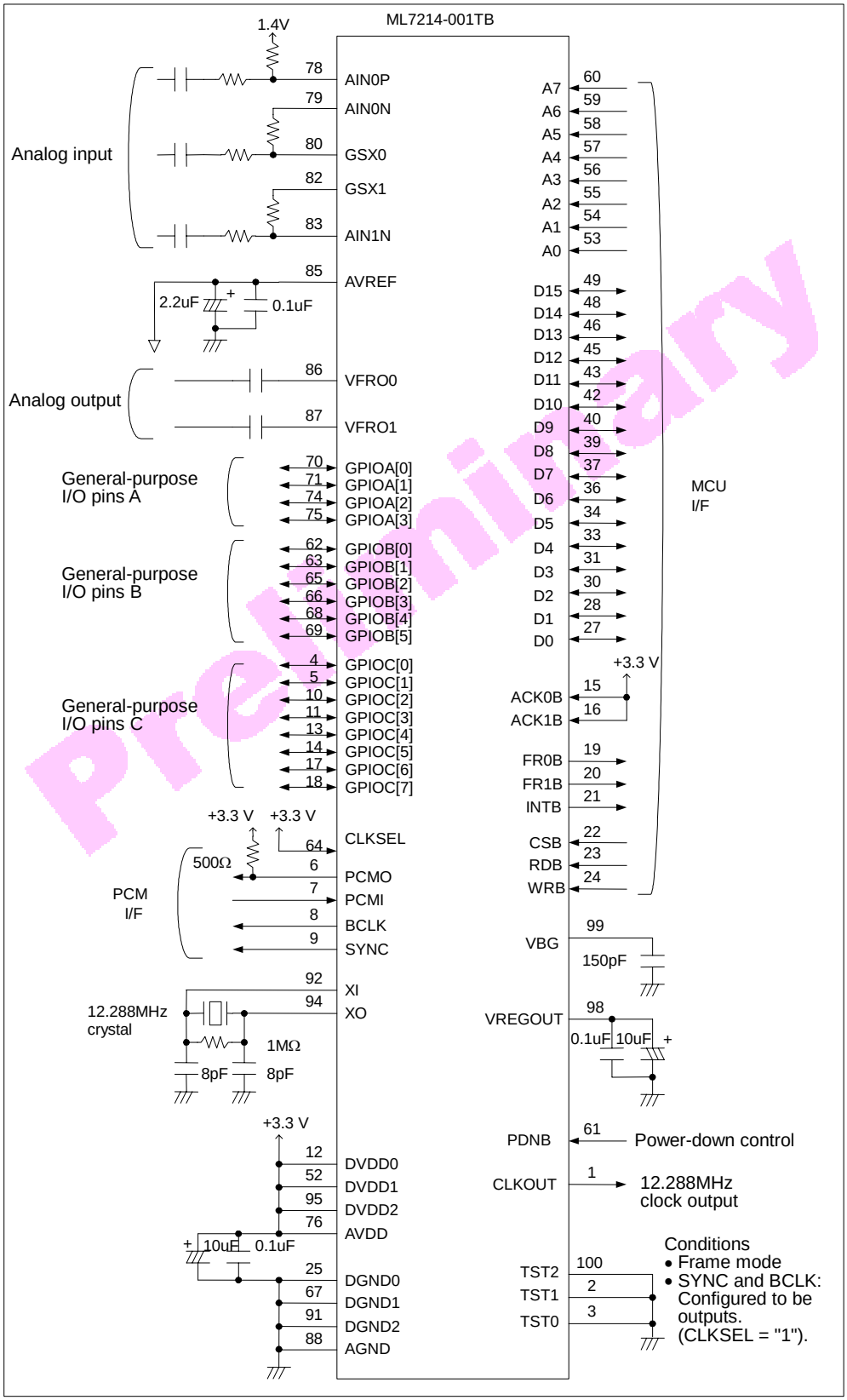
5. The initial values of the Speech CODEC selection register (TX_SCSEL[1:0]) on the transmit side and the Speech CODEC selection register (RX_SCSEL[1:0]) on the receive side are [0:0]. To use the Speech CODEC, be sure to set [0:1] (G.711 μ-law) or [1:1] (G.711 A-law) during the initial mode.

6. This LSL allows various types of path configuration by setting the speech path switch; however, the initial state of the speech path switch is all OFF. Set the speech path switch to ON according to usage, using the CH0 speech path control internal data memory (SWCONT_CH0) and CH1 speech path control internal data memory (SWCONT_CH1).

7. If two signals have been added according to the setting of the speech path switch, adjust the signal level using the gain controller inserted into the path before addition so that the signal level after addition will not exceed a maximum amplitude of 3.17dBm0.

8. Be sure to leave the NC pin (unused pin) open. Never connect it to the ground, power supply or other signal line.

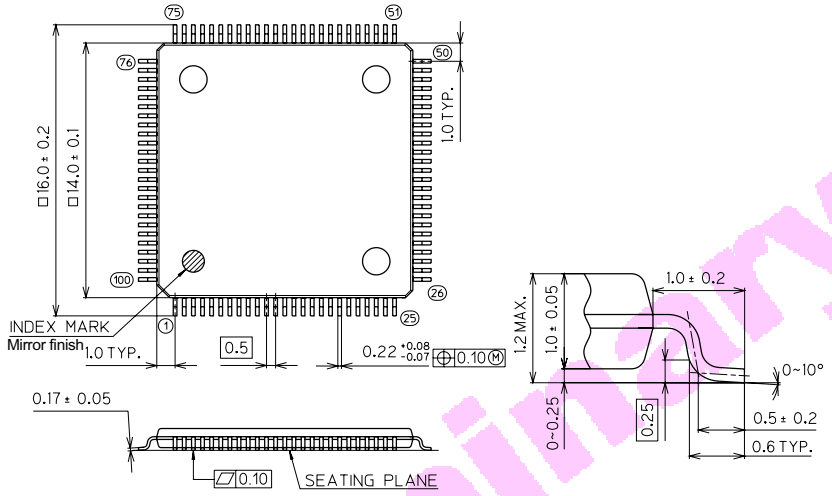
APPLICATION CIRCUITS



PACKAGE DIMENSIONS

(Unit: mm)

TQFP100-P-1414-0.50-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	0.55 TYP.
Rev. No./Last Revised	4/Oct. 28, 1996

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Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL7214_001DIGEST-P	Jan. 31, 2006	–	–	Preliminary edition 1

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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